

SB-USB

Universal DSP emulator

Rev. B

Product of Domain Technologies, Inc.

*SB-USB Rev. B User's Guide,
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1.1 - Overview of the SB-USB

SB-USB is a universal emulator capable to operate in multiple modes:

- Motorola JTAG - support for multiple JTAG devices
- Motorola OnCE - support for two OnCE DSPs (56000 and/or 56100)
- TI JTAG - support for multiple JTAG devices

Mode of operation is changed during system initialization, depending on selected options.



1.2 - Installation instructions

SB-USB can be installed on the PC computer with Windows 98 or Windows 2000. Windows 95 and Windows NT do not support USB devices.

After connecting SB-USB system to the USB port of the host computer, Windows will attempt to install device drivers for the USB peripheral. Drivers for the USB interface of the SB-USB are located on the CD in the respective directories:

- for Windows 2000: D:\Win2000
- for Windows 98/Me: D:\Win98

For TI devices, device driver needs to be installed from the included CD. The driver provides an access to the SB-USB from the Code Composer Studio. Driver by default is installed in the directory \ti\drivers and it is called dtiusb54.dvr. Driver is using another library - sbusbd32.dll installed in the "system" directory (\winnt\system32 or \windows\system). Please follow Code Composer Setup instructions for installing additional device drivers.

1.3 - BoxView interface

For access to the Motorola's DSPs BoxView debugger and BoxServer (multiple device access) need to be installed from the supplied CD.

For single target device emulator can be controlled directly by the BoxView software. For multiple devices connected in OnCE or JTAG mode, emulator needs to be controlled by the BoxServer application. Prior to launching BoxServer application, BoxServ.ini needs to be modified to reflect actual target configuration.

For the JTAG devices, Target1 is the device closest to the TDO pin of the emulator (last device on the scan-chain).

1.4 - Code Composer interface

For Texas Instruments' DSPs from C5400 family, SB-USB needs to be used with Code Composer development system. Code Composer Studio is available as an optional item, either from Domain Technologies or from Texas Instruments distributor. The SB-USB package contains a necessary driver, enabling access from the

Code Composer debug subsystem to the firmware of the SB-USB. The driver needs to be installed and selected through the Code Composer Setup application.

The SB-USB emulation driver is supplied as a "sbusb54.dvr". The driver needs to access dynamically loaded library (dll):

- sbusbd32.dll - main control for Domain's USB emulators

The CCS driver should be copied from the CD-ROM to the directory accessible by the Code Composer setup program (default one is c:\ti\drivers). The dll's should be copied into directory specified with the system path:

Win98/Me: \windows\system

Win2000: \winnt\system32

2.1 - SB-USB board

Main emulation connector is accessible from the outside of the box. There are also optional headers and configuration jumpers on top of the board. To change jumper settings, top cover needs to be removed - 4 screws on the bottom side of the enclosure. There are no components on the bottom side of the printed circuit board.

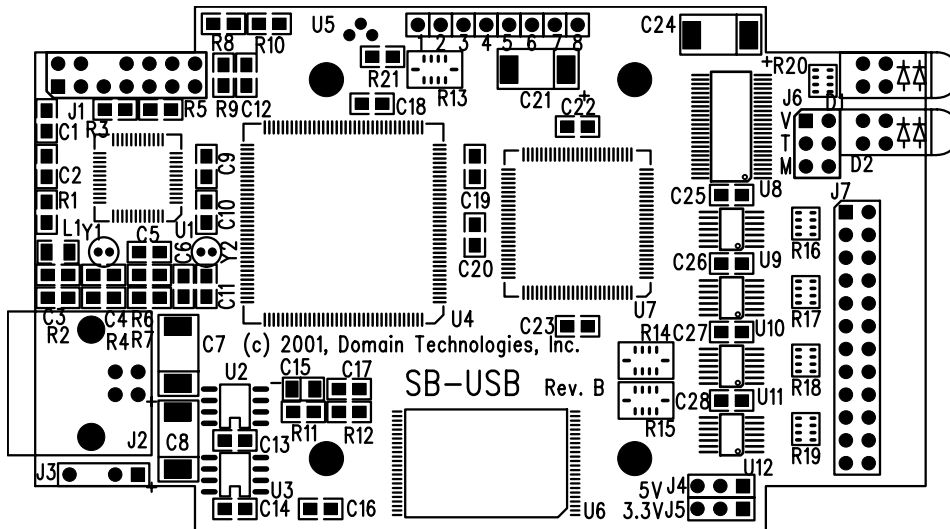


FIGURE 2.1. SB-USB board

2.2 - External connectors of the SB-USB

- J7 – Target emulation
- J2– USB connector

Right angle header J7 allows to connect to various hardware types. Pin functions are controlled by the micro controller. Three basic modes of operation are supported:

- Motorola OnCE - two independent connections
- Motorola JTAG
- TI JTAG

Pin assignment for each of the above modes is described in the following three tables.

TABLE 2.1. Pinout definition in the OnCE mode

Pin #	Signal	Pin #	Signal
1	DSI 0	2	Gnd
3	DSO 0	4	Gnd
5	DSCK 0	6	Gnd
7	-DR 0	8	Gnd
9	-RESET 0	10	nc
11	TrgVcc	12	nc
13	nc	14	nc
15	DSI 1	16	Gnd
17	DSO 1	18	Gnd
19	DSCK 1	20	Gnd
21	-DR 1	22	Out0/3.3V
23	-RESET 1	24	Out1/5V

TABLE 2.2. Pinout definition in Motorola JTAG mode

Pin #	Signal	Pin #	Signal
1	TDI	2	Gnd
3	TDO	4	Gnd
5	TCK	6	Gnd
7	nc	8	Gnd
9	-RESET	10	TMS
11	TrgVcc	12	TMS1
13	-DE	14	-TRST

TABLE 2.2. Pinout definition in Motorola JTAG mode

Pin #	Signal	Pin #	Signal
15	nc	16	Gnd
17	nc	18	Gnd
19	nc	20	Gnd
21	IN1	22	Out0/3.3V
23	IN0	24	Out1/5V

TABLE 2.3. Pinout definition in TI JTAG mode

Pin #	Signal	Pin #	Signal
1	TMS	2	-TRST
3	TDI	4	Gnd
5	PD	6	Gnd
7	TDO	8	Gnd
9	nc	10	nc
11	TCK	12	nc
13	EMU0	14	EMU1
15	nc	16	Gnd
17	nc	18	Gnd
19	nc	20	Gnd
21	IN1	22	Out0/3.3V
23	IN0	24	Out1/5V

2.3 - Light emitting diodes (LEDs):

D1 Bottom – OnCE #1/JTAG status

D1 Top – OnCE #2 status

D2 Bottom – operating mode

D2 Top – activity indicator

Top left led monitors state of the emulator micro controller. When idle, it constantly toggles this LED between red and green. If the firmware is not initialized, or controller is busy, this LED will stop toggling.

Bottom left LED indicates mode of the emulator operation:

blinking - not initialized
off - Motorola OnCE mode
red - Motorola JTAG mode
green - TI JTAG mode

For JTAG modes bottom right LED indicates last change of the target state:

off - device in user mode
red - device halted with software breakpoint or halt command
green - device halted with hardware breakpoint, or single step

In JTAG mode upper right LED is not used.

In OnCE mode, lower right LED shows state of the first device, and upper right shows the state of the second device:

off - device in user mode
red - device halted with software breakpoint or halt command
green - device halted with hardware breakpoint, or single step

2.4 - Internal connectors and jumpers:

J5 – OUTPUT0, 3.3 V supply selection
J4 – OUTPUT1, 5 V supply selection
J1 – JTAG access
J6 – I/O buffer supply selection
J3 – External power supply

Three pin header J5 allows to select mode of the pin 22 of the external connector J7. In the default configuration, this pin is connected to the control output 0 - normally tristated. Setting the jumper on pins 2 and 3 (towards back of the device), will connected emulators 3.3V. Maximum current drawn by the target can be 150 mA.

The header J4 has the similar function, as header J5. It allows to select between control output 1 and 5 V. Maximum current - 150 mA.

Header J3 can provide external power to the system. It is used only during manufacturing, and the jumper should be set on pin 1 and 2 (toward front) all the time.

Header J1 is also used only during manufacturing process for initial programming of the flash ROM. It provides external emulator access to the control processor.

Header J6 allows selection of different I/O voltages for the external I/O buffers. By default the jumper is set on pins 1 and 2, labeled with letter 'V'. This connects supply to the internal 3.3V of the SB-USB.

For target devices requiring lower I/O voltage on the emulation pins, buffers can be supplied with external source.

Pins 3-4 ('T' label) connect supply to pin #5 of the external emulation header. This is standard pin location for TI's DSP emulation header.

Pins 5-6 ('M' label) connect supply to pin #11 of the external emulation header. This is standard pin location for Motorola's DSP emulation header.

“Block Diagram” on page 16

“Emulation control” on page 17

“CPU, Memory” on page 18

“USB interface” on page 19

“Power, LEDs” on page 20

“Quad JTAG adaptor” on page 21

“PROBE-56001” on page 22

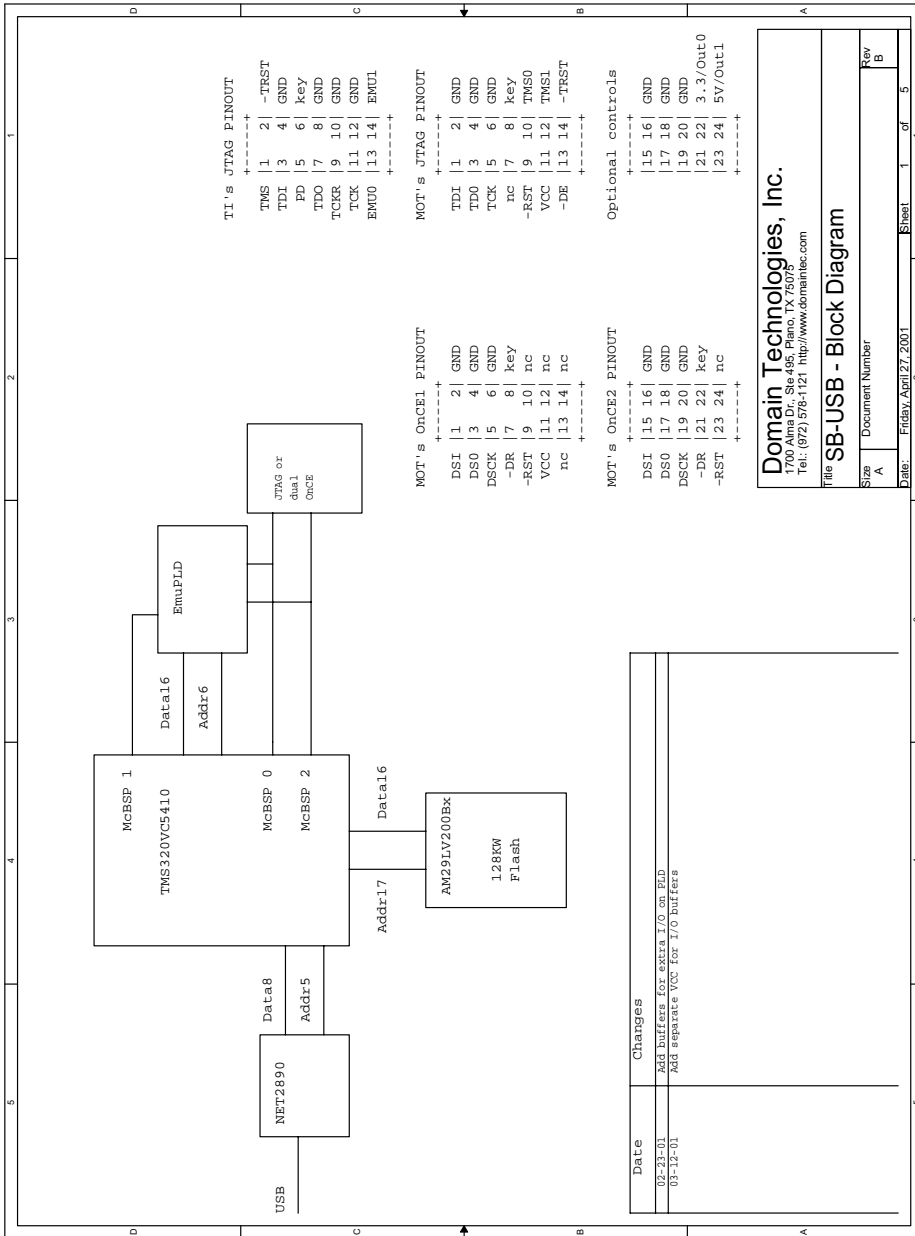
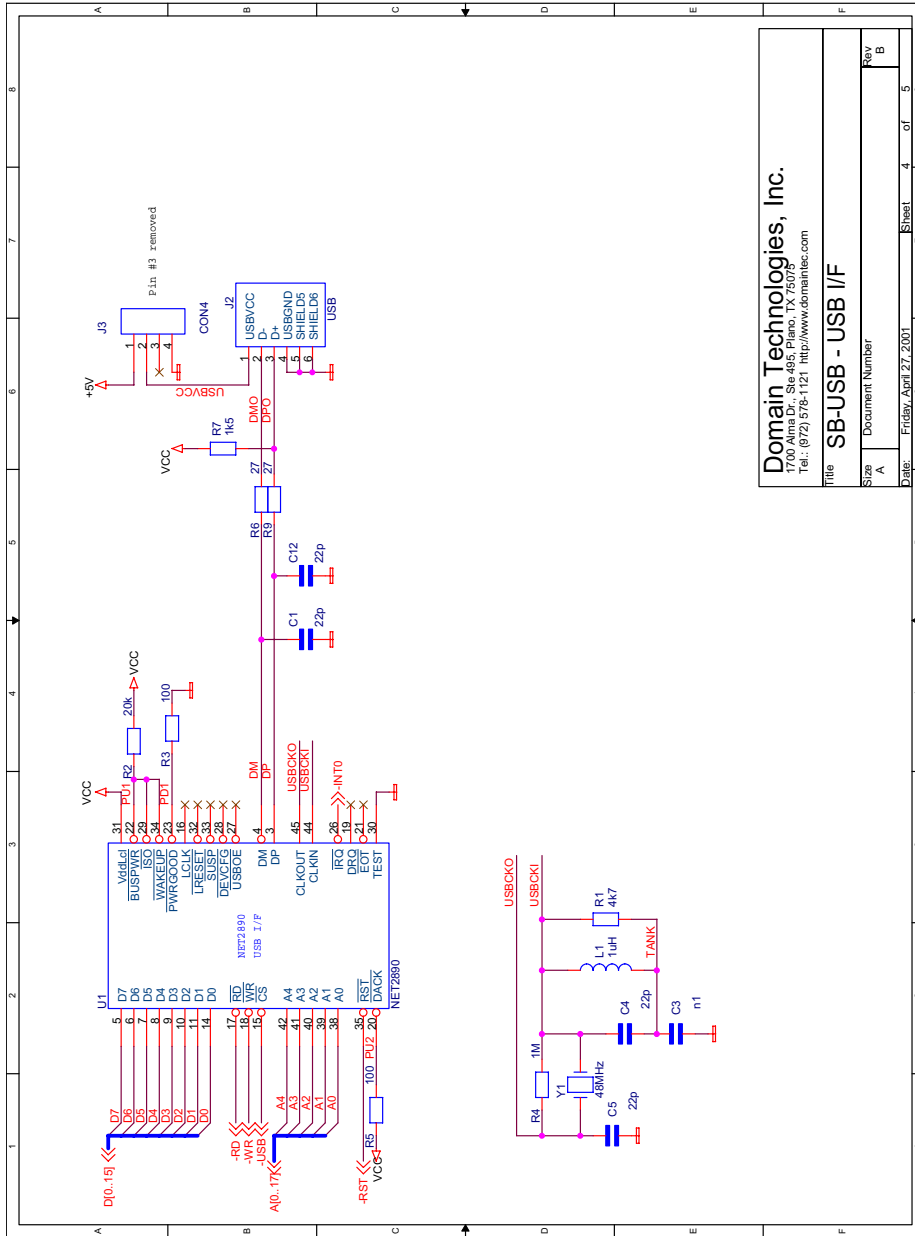


FIGURE 3.1. Block Diagram



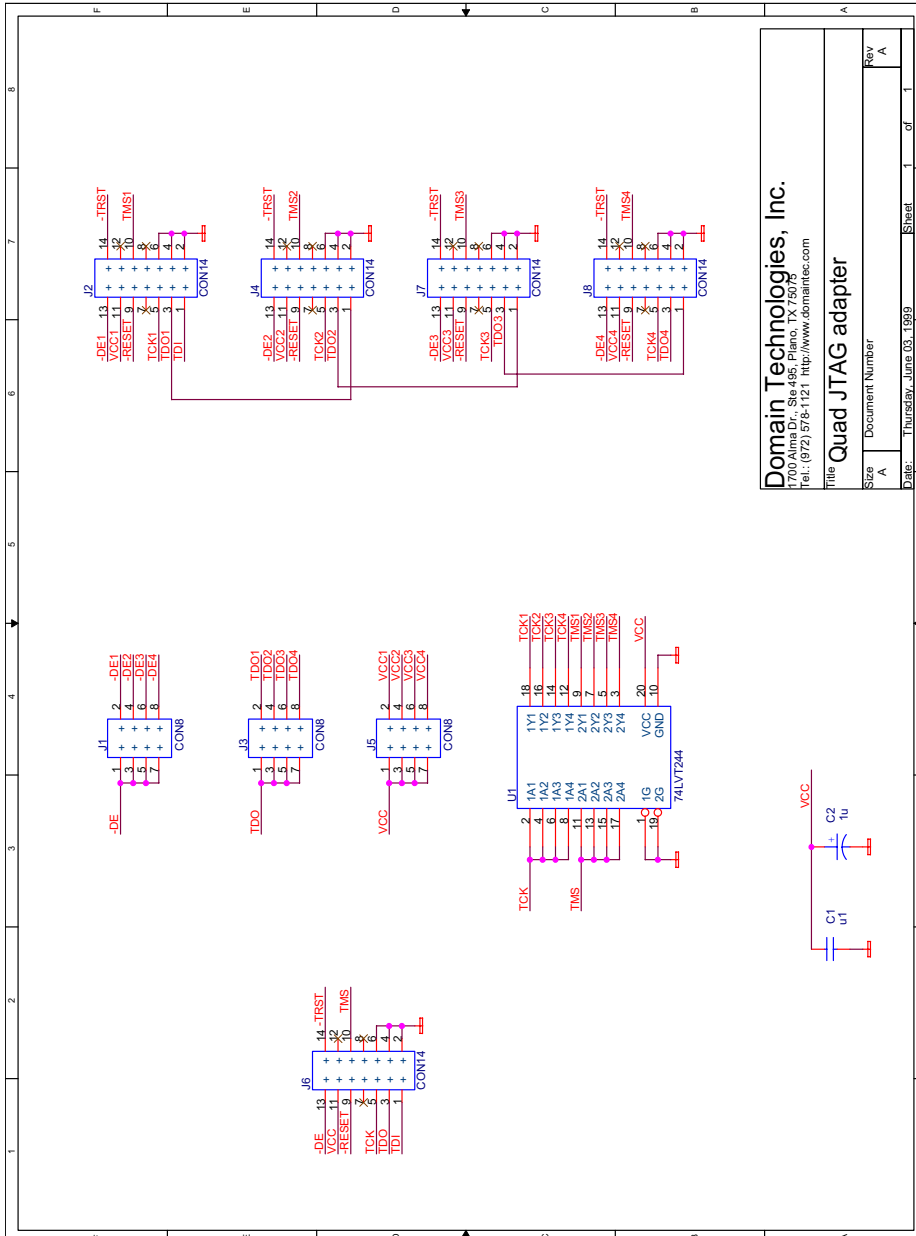


FIGURE 3.6. Quad JTAG adapter

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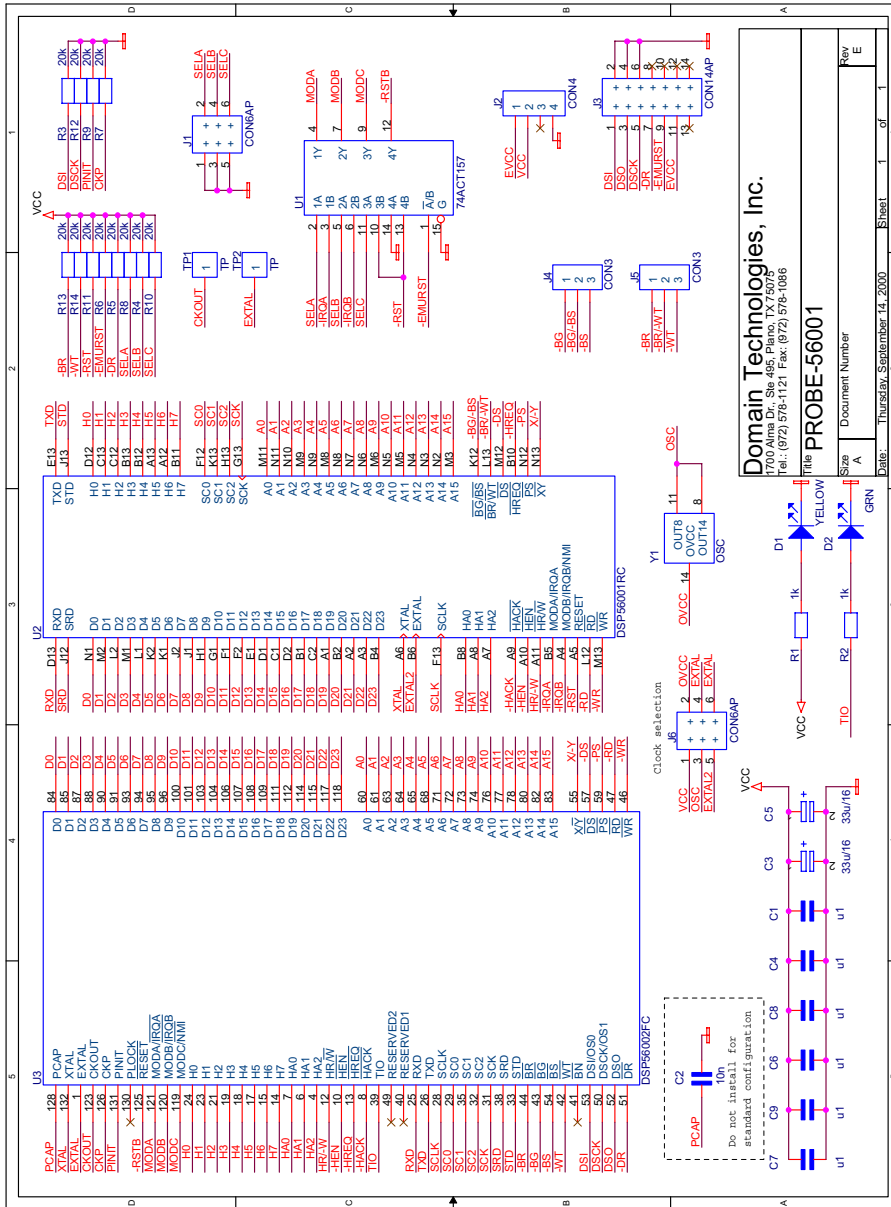


FIGURE 3.7. PROBE-56001

3.1 - PLD Registers

Emulation control registers are located in the PLD within the I/O memory space of the control CPU.

Addresses form 0 to 0x1f are reserved for the USB interface controller access.

TABLE 3.1. Address 0x20 – LED Control, control signals – outputs only R/W

Bit #	Function	Pin #	Signal
0	LED0	8	DRA
1	LED1	9	DRB
2	LED2	10	RSTA
3	LED3	11	RSTB
4	LED4	12	CTRL0
5	LED5	13	CTRL1
6	LED6	14	
7	LED7	15	

TABLE 3.2. Address 0x21 – Control signals R/W

Bit #	Function	Pin #	Signal
0	ENACTRL	8	TJTAG
1	ENAEMU0	9	MJTAG
2	ENAEMU1	10	MCTRL
3	ENATRST	11	
4	ENATMS0	12	OUT_0
5	ENATMS1	13	OUT_1
6	ENATCKR	14	IN_0
7	ENAJTCK	15	IN_1

TABLE 3.3. Address 0x22 – Status, latch and mask register

Bit #	Function	Pin #	Signal
0	BDR0 Mask	8	OS0A
1	BDR2 Mask	9	OS1A
2	EMU0 Mask	10	OS0B/EMU0
3	EMU1 Mask	11	OS1B
4	BDR0 Latch	12	EMU1
5	BDR2 Latch	13	MPD
6	EMU0 Latch	14	
7	EMU1 Latch	15	

TABLE 3.4. Address 0x23,24 - Counter 0/1 Control

Bit #	Start source	Pin #	Stop source
0	BFS0 v	8	BDR0 v
1	BFS2 v	9	BDR2 v
2	BDX2 ^	10	EMU0 v
3	-RSTA ^	11	EMU1 v
4	EMU0 ^	12	EMU0 ^
5	EMU1 ^	13	EMU0 ^
6	EMU0 v	14	
7	EMU1 v	15	

TABLE 3.5. Address 0x26/28 – Timer/Counter control register 0/1

Bit #	Function	Description
0	Auto reload	If 1 - counter reloads with reload register value. If 0 - underflows to \$FFFF and continues
1	Auto Re-Arm	If 1 - counter will continue counting through multiple start/stop sequences after initial Arm
2	Counter Mode	If 0 - timer mode, which starts down counting after start trigger until stop trigger If 1 - counter mode, which counts stop trigger active edges after initial start trigger
3	Enable	If 1 - counter is enabled If 0 - counter is disabled and clears Arm
4	Int enable	If 1 - Counter Interrupt enable flag
5	Arm/Armed	Write 1 to Arm, read back to see if still armed
6	Started	If 1 - counter started (read only)
7	Int pending	Counter counted to zero with Int enable flag set. Cleared automatically after status read.

Address 0x27 and 0x29:

Read - current count value

Write - load reload register and the counter register

Address 0x2A

PLD version

