

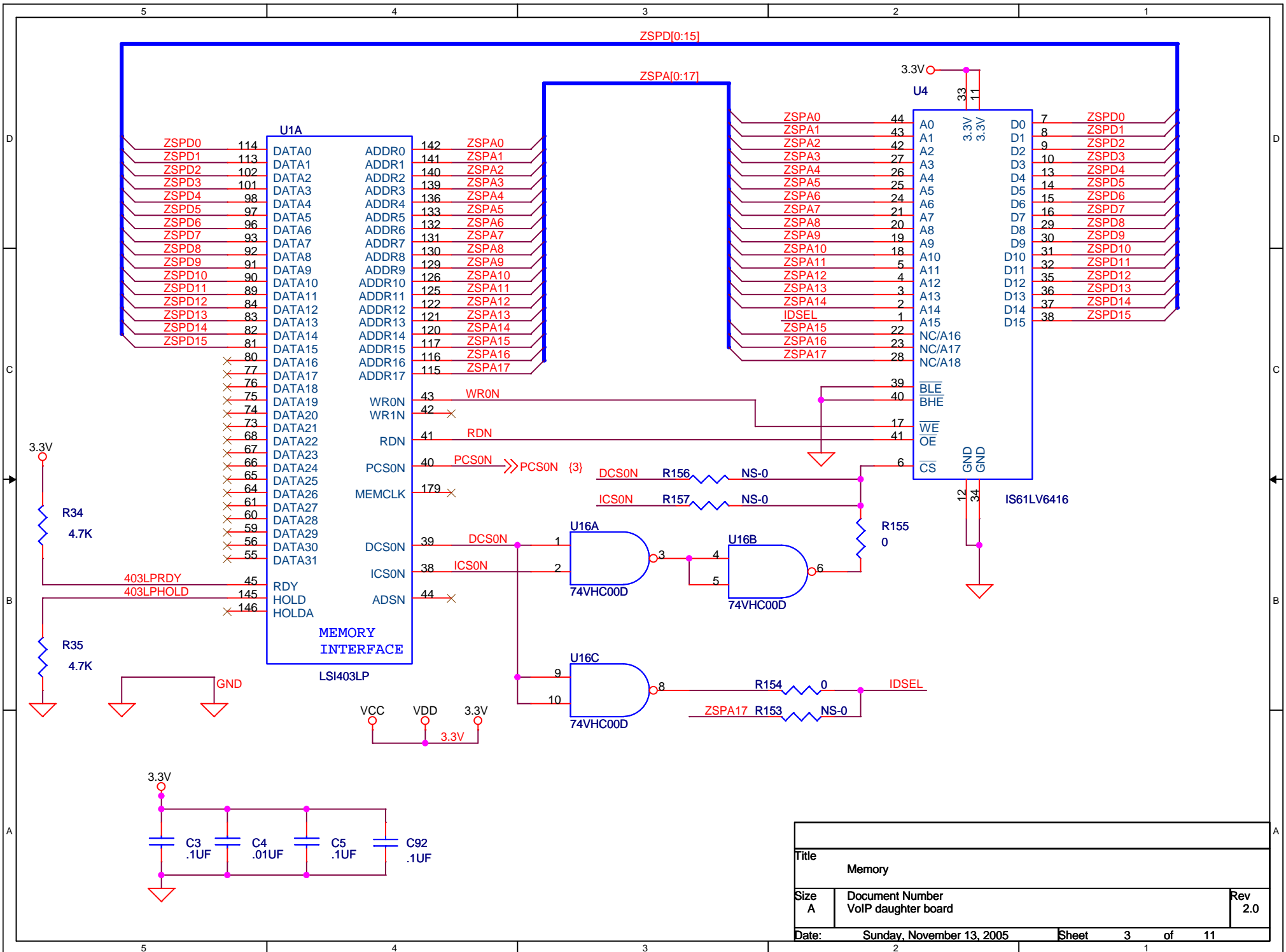
REVISION HISTORY

DATE:	DESCRIPTION	REVISION
6/28/04	INITIAL RELEASE	1.0
7/6/04	Release to PCB LAYOUT	1.1
7/7/04	UPDATE CHNAGES PER LSI LOGIC INPUT	1.2
7/12/04	ADD DECOUPLING CAPS FOR 3.3VOICE	1.3
9/14/05	PEK - Add decode for I/D Sram sel (U16), chg JP3 form 10 pin to 14 pin, add TP5,6 for HOBE/HOBIB conn to J1	1.4
	Remove R36, R37, add U14 (403LC), U16 (00), C92	
10/08/05	PEK - Add FXO circuit, HPI header, power supply, power test points	2.0
10/14/05	Change PLLSEL to b1101. Put note about misconnect of pin 152 (403LP), 403LC only TAVDD conn to 1.2VPLL	
	Add LED to PIO0, HPI mode select pullups for PIO1, add jumper for IBOOT	

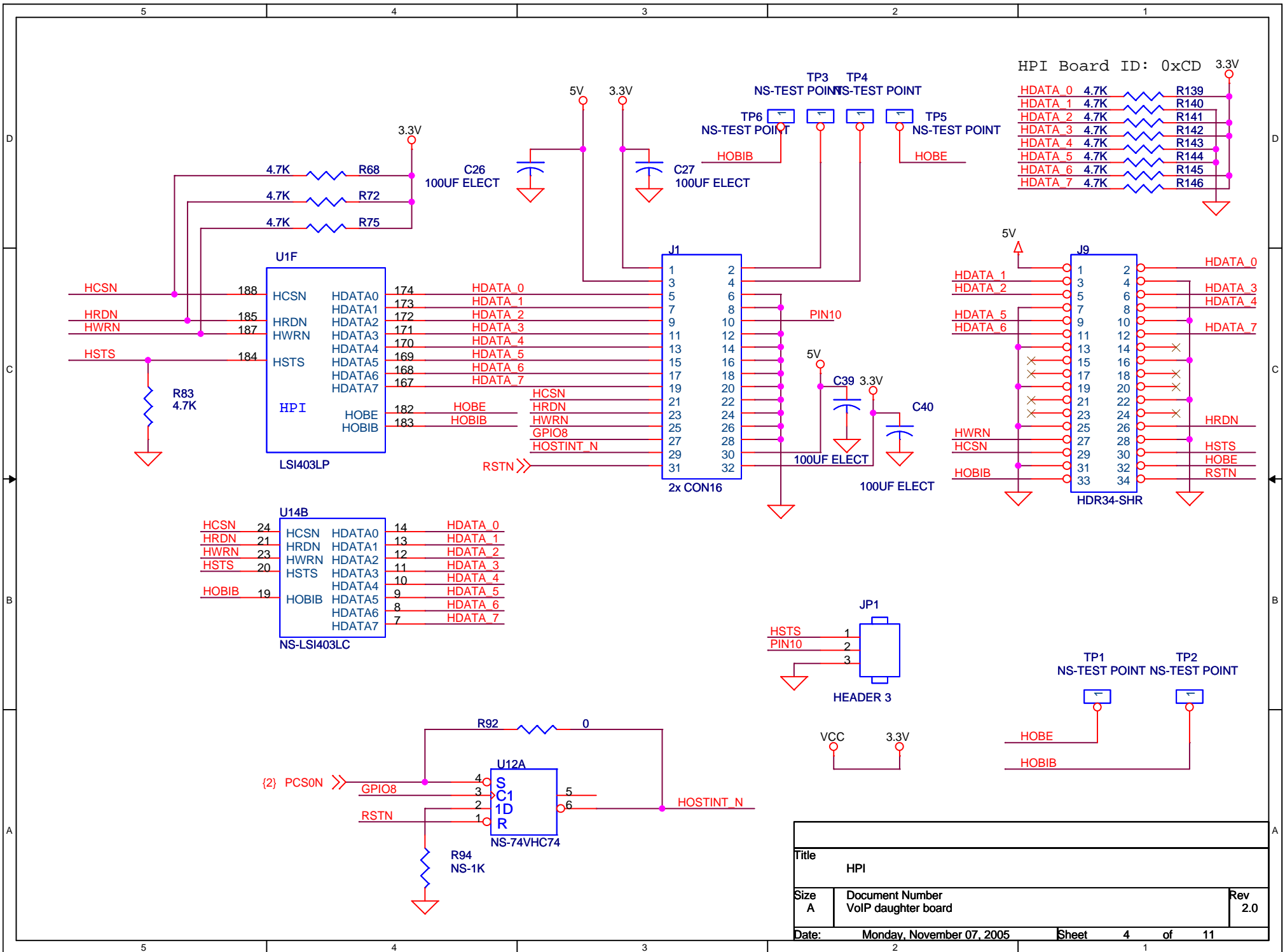
Page 1: Revision history                      Page 7: SLIC2  
 Page 2: System interface                    Page 8: SLIC 2, Lines 3 and 4  
 Page 3: Memory                                Page 9: SLIC power, JTAG  
 Page 4: Host port interface                Page 10: FXO  
 Page 5: SLIC 1                                 Page 11: Power  
 Page 6: SLIC 1, Lines 1 and 2

Title		
REVISION HISTORY		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 1 of 11

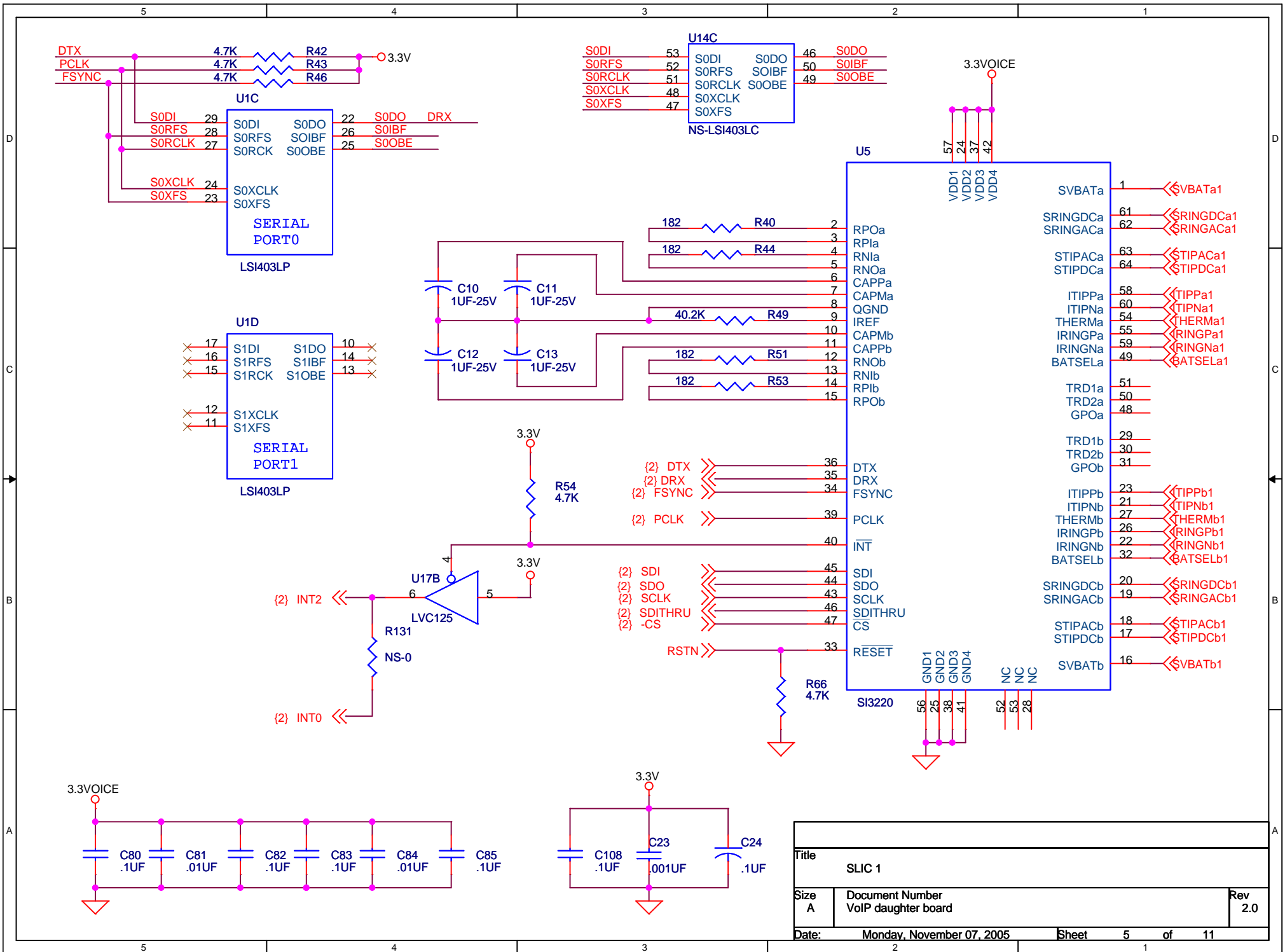




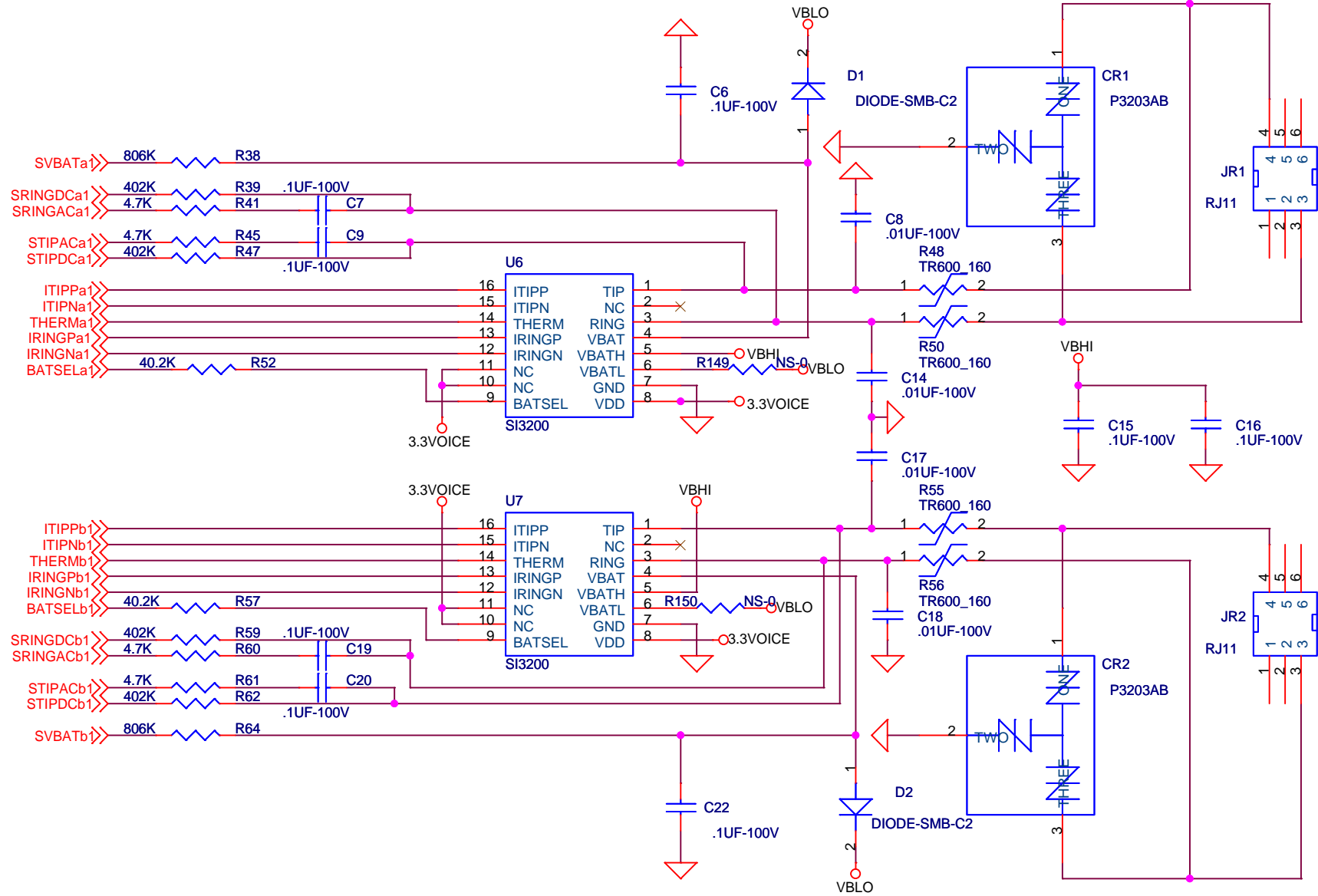
Title		
Memory		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Sunday, November 13, 2005	Sheet 3 of 11



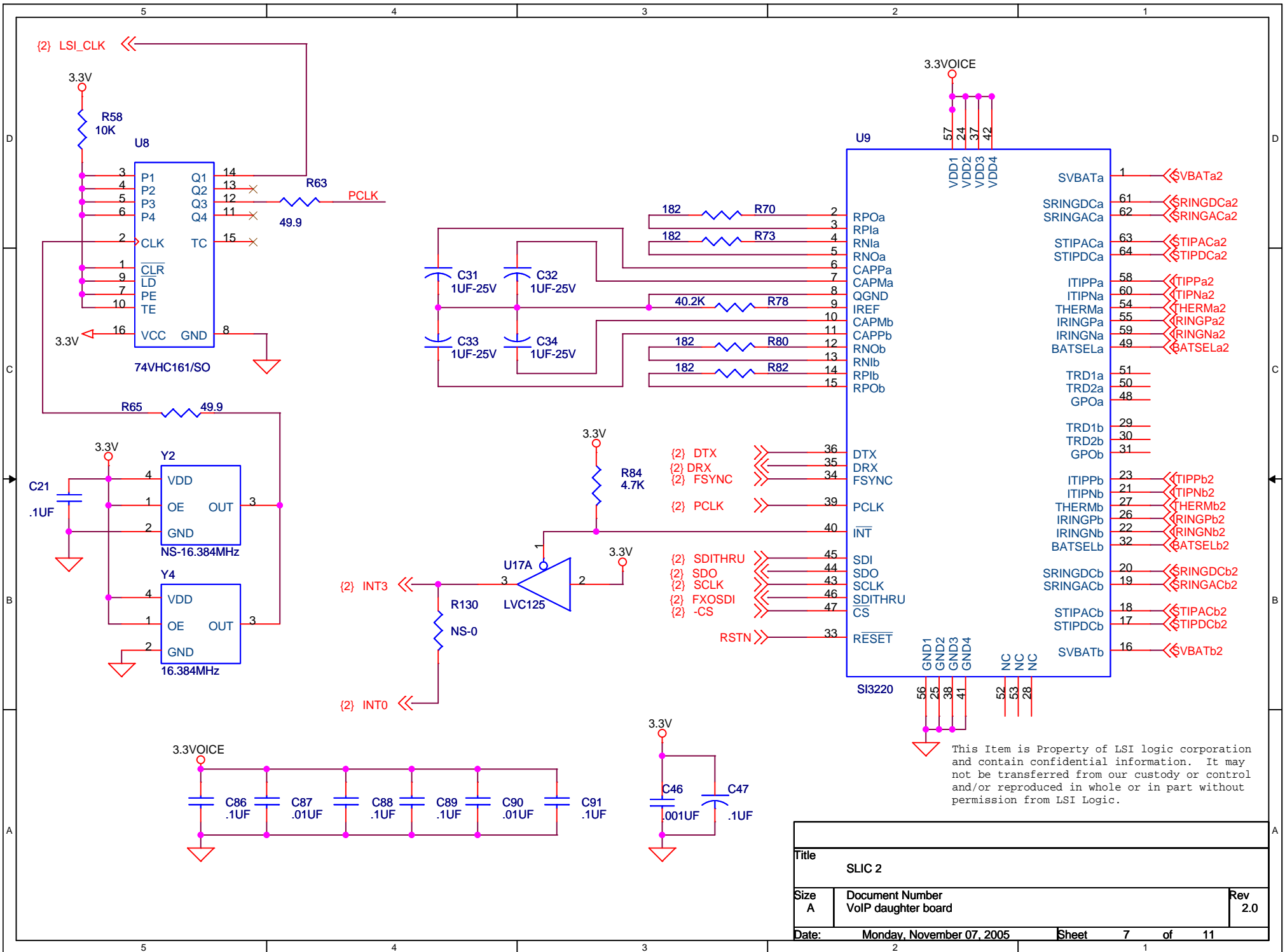
Title		
HPI		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 4 of 11



Title		
SLIC 1		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 5 of 11

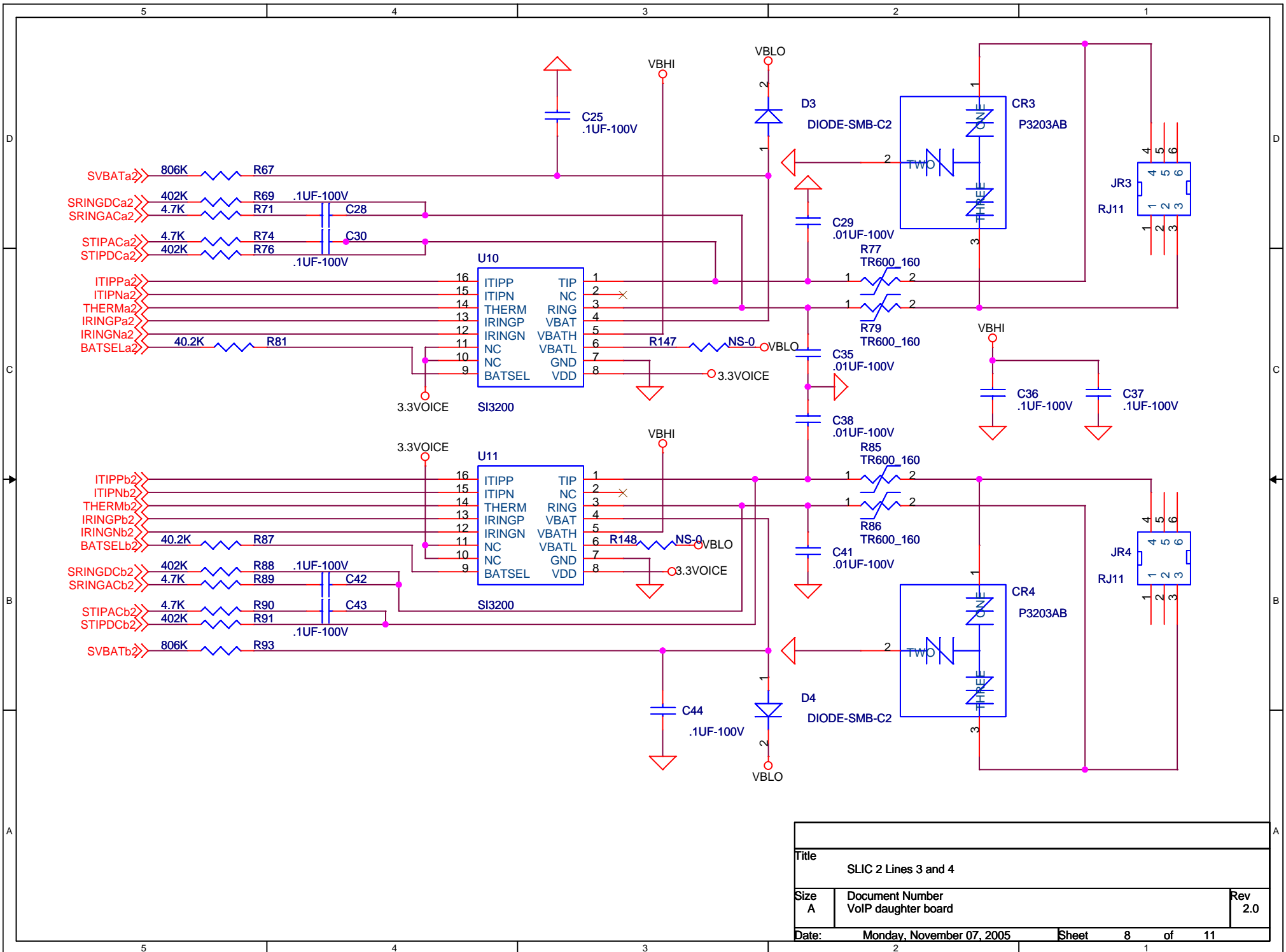


Title		
SLIC Lines 1 and 2		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 6 of 11

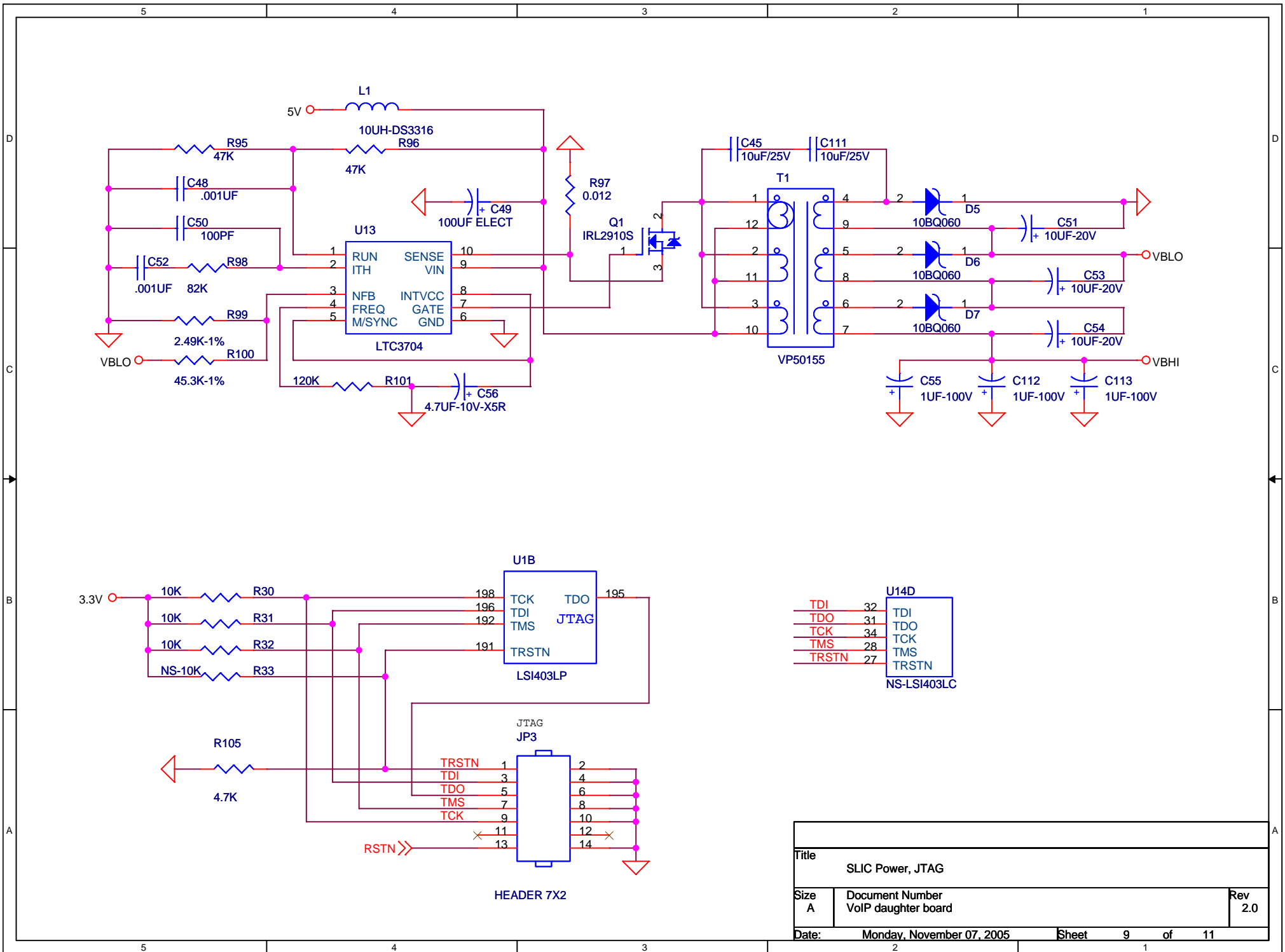


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Title		
SLIC 2		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 7 of 11

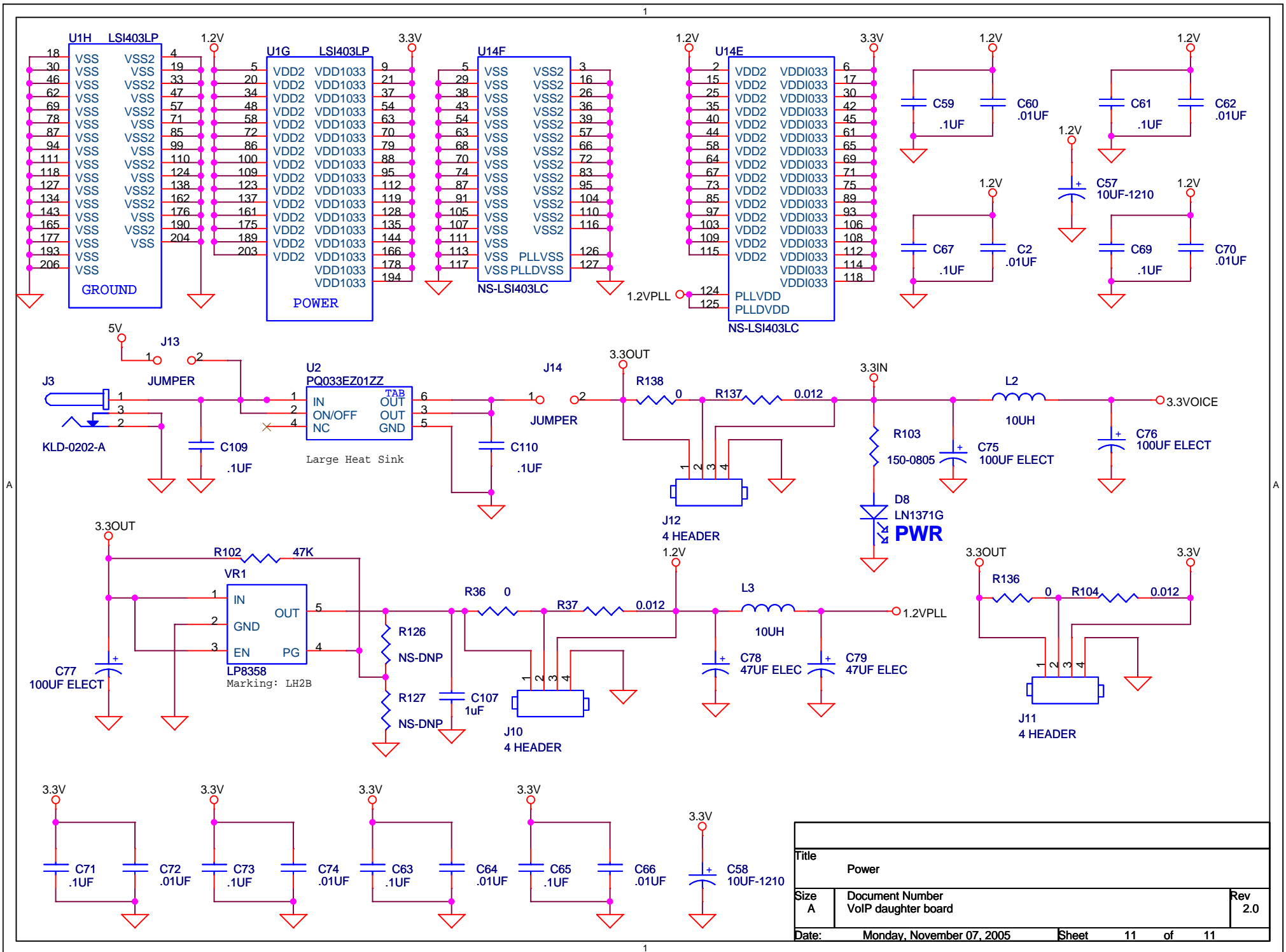


Title		
SLIC 2 Lines 3 and 4		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 8 of 11



Title		
SLIC Power, JTAG		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 9 of 11





Title		
Power		
Size	Document Number	Rev
A	VoIP daughter board	2.0
Date:	Monday, November 07, 2005	Sheet 11 of 11