

DTSP3EB User Guide

Quick Start

1. Install software from the supplied CD. If the CD is not available, download latest installation program from Domain Technologies' web site:

<http://www.domaintec.com/zspsoftware.html>

The Installation files are also available on the FTP:

<ftp://ftp.domaintec.com/zsp/DtiZspInstall.exe>

Installing software before connecting the hardware to the PC's USB port provides Windows with information about the location of the USB drivers.

2. Connect +5V DC to the power connector. The power LEDs will be turned on, and USB microcontroller status LED number 1 will be blinking.
3. Connect USB cable between the host computer and the evaluation board. If the USB port of the PC is connected for the first time, it will install the drivers for the DTSP3EB board. Connecting to another USB port will cause driver installation again, which is normal.
4. Initialize FPGA by executing the DTSP3INIT.EXE application. At this point the middle eight status LEDs should start scrolling from bottom to top. This indicates that the ZSP is initialized on the FPGA and software monitor code is executing.
5. Start BoxView or sdebug400, load demo application lddemo.out, and get started.

Device initialization.

The FPGA on the evaluation board is not programmed and requires initialization through the USB port. The fastest way to load the logic to the FPGA is by the console application DTSP3INIT.EXE. After that, an external JTAG emulator can be connected. Alternatively, BoxView, the ZSP IDE, or sdebug400 could be used alongside mdidtsps3.dll to program the FPGA.

To use with BoxView;

1. Select Options->Open Connections
2. Choose DTSP3EB for the interface type and click OK
3. After connecting, choose Process->Reset to initialize the FPGA.

To use with ZSP IDE:

1. Load a project
2. Select Debug->Settings
3. Choose an editable JTAG debug profile (may need to choose "save as.." to create one) and change "debug command" to:
`sdebug400 --mdi_library=mdidtsps3.dll`
4. Choose Debug->Run

To use with sdebug400:

1. Invoke on the command line with:

- ```
sdebug400 -mdi_library=mdidtsp3.dll
```
2. Connect with the command  
target jtag

For the initialization process succeed, the following jumpers must be installed:

J2 connecting pins 2 and 3. This bypasses the JTAG port of the configuration device, which is not installed.

J7 connecting pins 3 and 4 (CLK11→CLKIN) – on board clock oscillator connected to the FPGA clock input.

J26 slide switch on the TDO-ZSP side. The TDO-XLX side is always connected, and the TDO-ZSP connects JTAG's TDO signal output from the ZSP to the JTAG emulation circuitry.

SB1 switch position 5 - off. IBOOT signal needs to be in the high state, allowing bootstrapping software monitor through the JTAG port.

## FPGA logic configuration

Device is initialized in two steps. First, FPGA logic is uploaded from the STAPL file by the built in JAM file player.

The logic is uploaded from the external STAPL file through the FPGA's JTAG port. The procedure for selecting the STAPL file to be uploaded is as follows:

1. Read environment variable ZSP\_STAPL. If it is defined, check if the specified file can be opened.
2. Try to open file dtsp3eb.stapl in the current working directory.
3. Read environment variable BV\_HOME and try to open file in the config subdirectory:  
%BV\_HOME%\config\dtsp3eb.stapl
4. If none of the files can be opened, initialization ends with error.

Following logic upload, the software monitor is uploaded through the ZSP JTAG port, which is selected by the JTAG multiplexer, MUX control signal. MUX signal is automatically controlled by the microcontroller. The high level (MUX 1, Mux LED off) enables access to the FPGA, the low level (MUX 0, Mux LED on) enables access to the ZSP's JTAG port. The binary file selection with the monitor image is selected in a similar way:

1. Read environment variable ZSP\_BIN. If it is defined, check if the specified file can be opened.
2. Try to open file dtsp3eb.bin in the current working directory.
3. Read environment variable BV\_HOME and try to open file in the config subdirectory:  
%BV\_HOME%\config\dtsp3eb.bin
4. If none of the files can be opened, the default monitor image is uploaded into the ZSP

## ZSP debugging options.

ZSP debugger can only operate in software mode, by interacting with the monitor code loaded into low memory, between 0x0000 and 0x03FF. The default ZSPneo memory configuration provides 32 K words of instruction RAM (0x0000..0x7FFF), with the first 0x400 words reserved for the monitor, and 4 K words of data RAM (0x0000..0x0FFF). Top of the stack has to be less than 0x1000 – top of the stack is reserved for file I/O. Uploading program to the area between 0x0000 and 0x03FF will corrupt the monitor code. Repeat the entire initialization procedure to restore the monitor code.

Debugger can operate either through built-in JTAG controller, or through the external JTAG emulator. The built-in micro controller has limited program memory, and can support only low level JTAG debugging commands, which could be slower than the external JTAG emulator. The built-in JTAG controller supports the ZSP IDE and the sdebug400.exe (gdb debugger) by specifying the command line option: --mdi\_library=mdidtsps3.dll

## Default ZSPneo peripherals

**LEDs** are driven directly by the FPGA. The LED latch is implemented at the ZSP external data memory address 0x0008. The bit value 1 outputs to the external pin signal low, causing the corresponding LED to be switched on.

**LCD controller** is implanted as a latch at the external data address 0x0004. Low 8 bits are driving 8 data lines of the LCD display. Bit 8 (0x0100) is a R/-W control, currently not implemented, only writes to the LCD controller are possible. Bit 9 (0x0200) is LCD's RS signal, low value selects control, high value accesses displayed data. Bit 10 (0x0400) is LCD's E control signal, active high, after access operation is finished, all control bits should be cleared. Example of the LCD access is provided in the sample program: lcddemo.c

**Push button switches.** The current value of the push button switches can be read from the external data memory 0x80. Low four bits represent pressed switches F1..F4.

**Reset switch** causes the ZSP to go to the monitor bootstrap code. From the BoxView debugger, monitor code can be uploaded with the BOOTJTAG command.

Sequence of the BoxView commands to be executed to reinitialize monitor code:

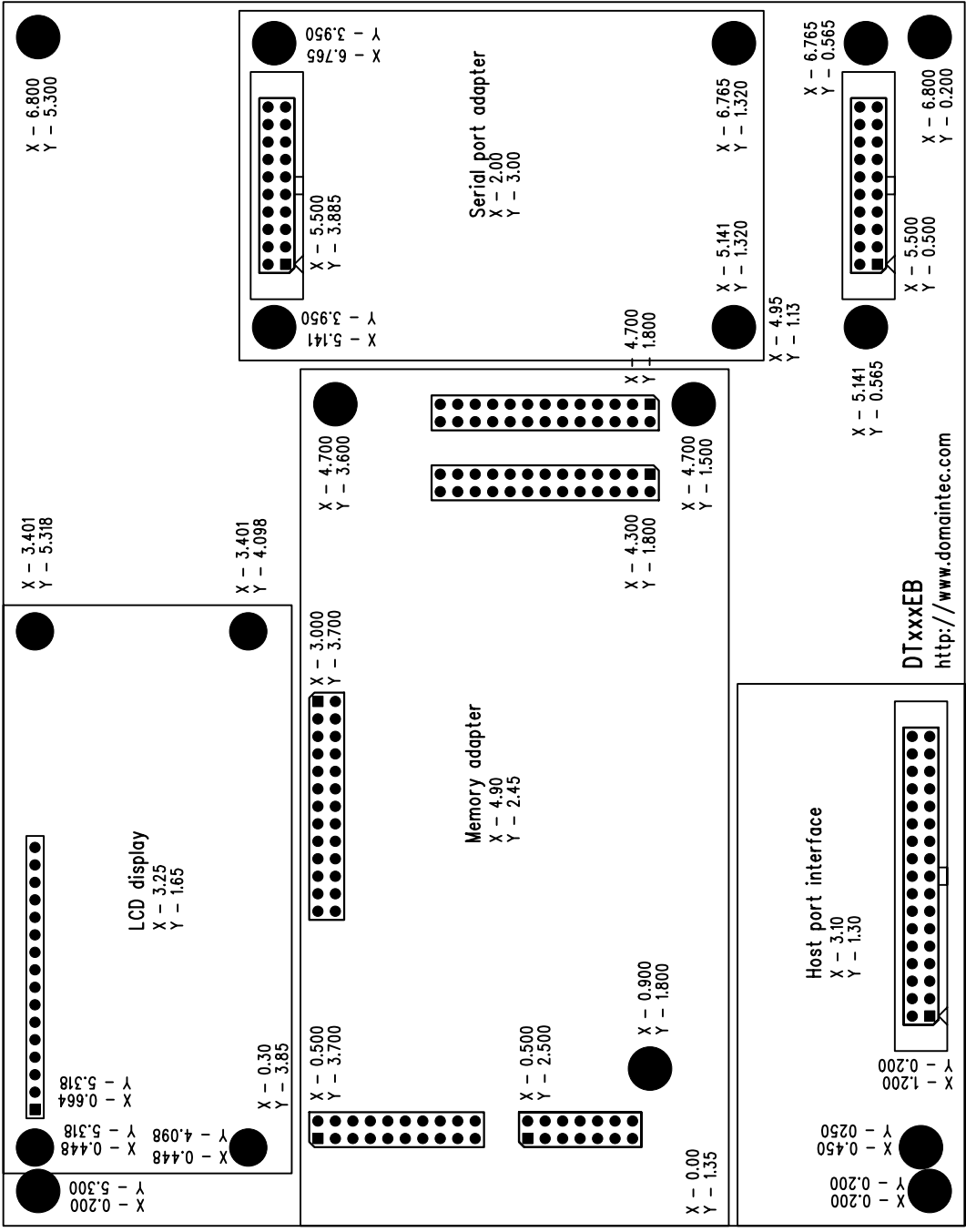
```
STATUS off ;disables checking of the monitor handshake flag (EX)
MUX 0 ;enables ZSP's JTAG access
;-- press RST switch to initialize JTAG bootstrap mode
BOOTJTAG ;command loads default monitor, or from specified file
STATUS on ;reenable status checking
```

BoxView debugger also provides complex command RESET, which will reload the FPGA image, then reload the software monitor code through the JTAG bootstrap process.

## DTSP3EB - mechanical specifications

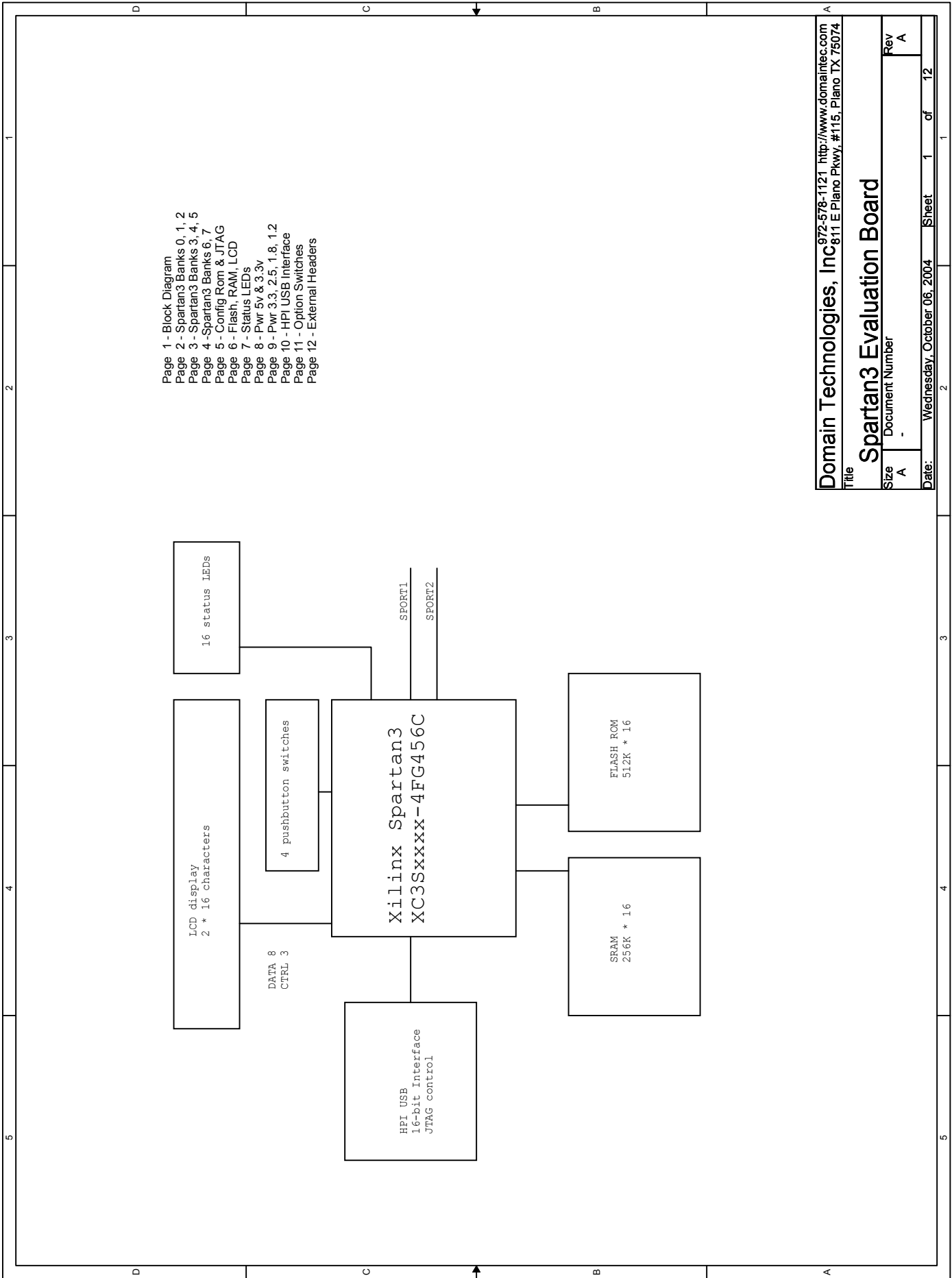
The following page illustrates location of all mounting holes, and recommended sizes for the board optional adapters. The location of the interface headers is provided by the location of the pin #1 of each header. Most of the interface headers are located on the 0.100" grid.

X - 7.000  
Y - 5.500



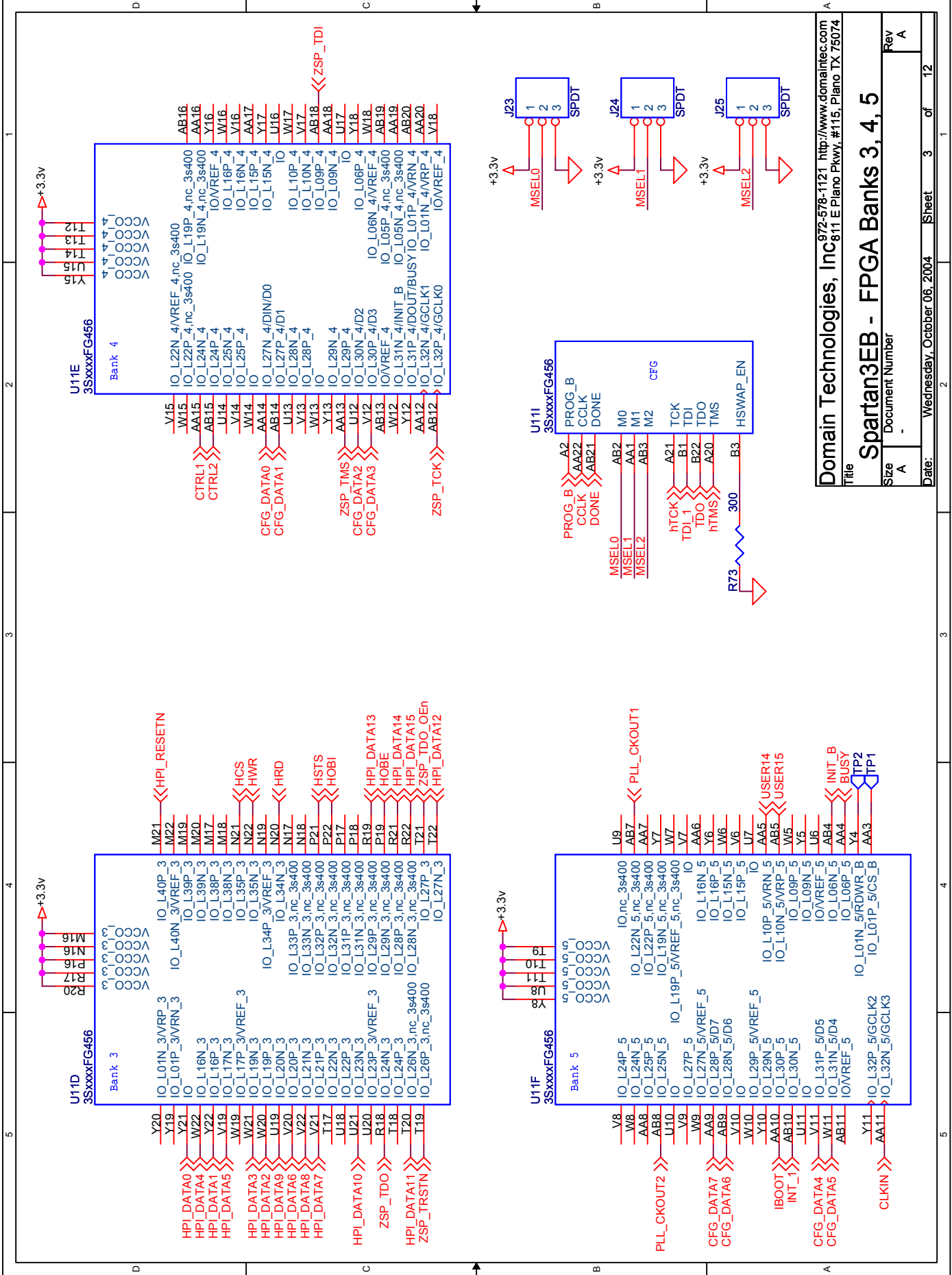
DTxxxEB  
<http://www.domaintec.com>

X - 0.000  
Y - 0.000



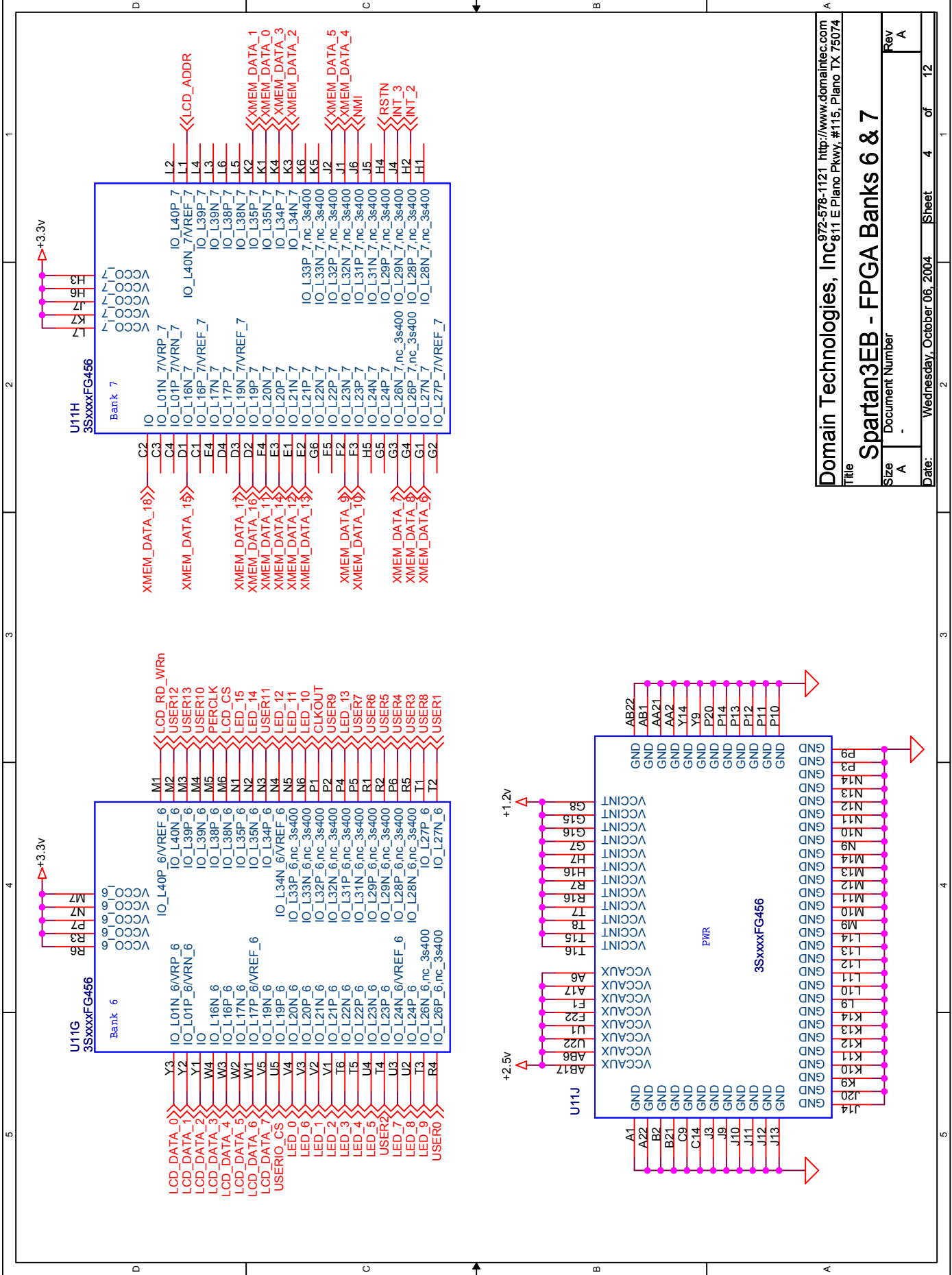
Page 1 - Block Diagram  
 Page 2 - Spartan3 Banks 0, 1, 2  
 Page 3 - Spartan3 Banks 3, 4, 5  
 Page 4 - Spartan3 Banks 6, 7  
 Page 5 - Config Rom & JTAG  
 Page 6 - Flash, RAM, LCD  
 Page 7 - Status LEDs  
 Page 8 - Pwr 5v & 3.3v  
 Page 9 - Pwr 3.3, 2.5, 1.8, 1.2  
 Page 10 - HPI USB Interface  
 Page 11 - Option Switches  
 Page 12 - External Headers



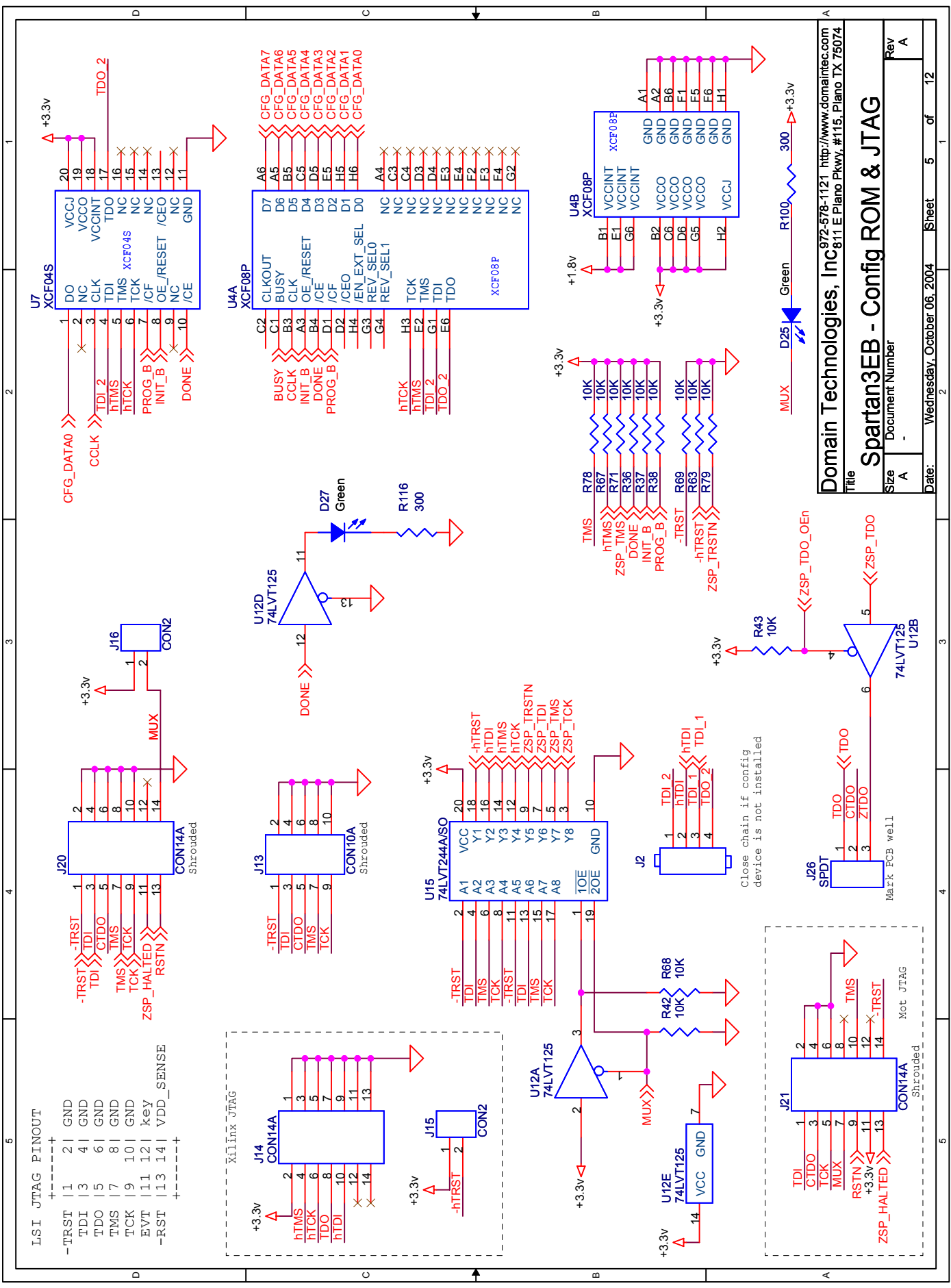


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|-------------------------------------------------------------------------------------------------------|------------------|
| Domain Technologies, Inc 972-578-1121 <a href="http://www.domaintec.com">http://www.domaintec.com</a> |                  |
| File: Spartan3EB - FPGA Banks 3, 4, 5                                                                 |                  |
| Size: A                                                                                               | Document Number: |
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|      |            |        |
|------|------------|--------|
| U11D | 3SxxxFG456 | Bank 3 |
| U11E | 3SxxxFG456 | Bank 4 |
| U11F | 3SxxxFG456 | Bank 5 |

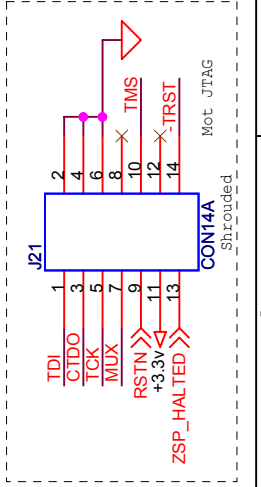
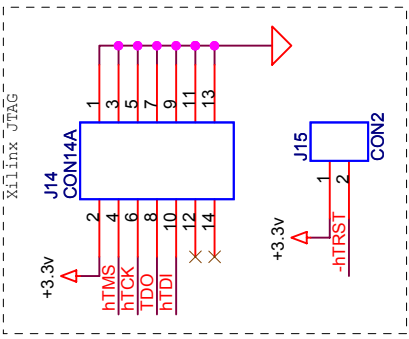


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| 811 E Plano Pkwy, #115, Plano TX 75074                                                                |                                          |
| <b>Title</b>                                                                                          | <b>Spartan3EB - FPGA Banks 6 &amp; 7</b> |
| <b>Size</b>                                                                                           | Document Number                          |
| <b>Rev</b>                                                                                            | A                                        |
| <b>Date:</b>                                                                                          | Wednesday, October 06, 2004              |
| <b>Sheet</b>                                                                                          | 4 of 12                                  |



ISI JTAG PINOUT

|       |    |    |           |
|-------|----|----|-----------|
| -TRST | 1  | 2  | GND       |
| TDI   | 3  | 4  | GND       |
| TDO   | 5  | 6  | GND       |
| TMS   | 7  | 8  | GND       |
| TCK   | 9  | 10 | GND       |
| EVT   | 11 | 12 | key       |
| -RST  | 13 | 14 | VDD_SENSE |



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Title: Spartan3EB - Config ROM & JTAG

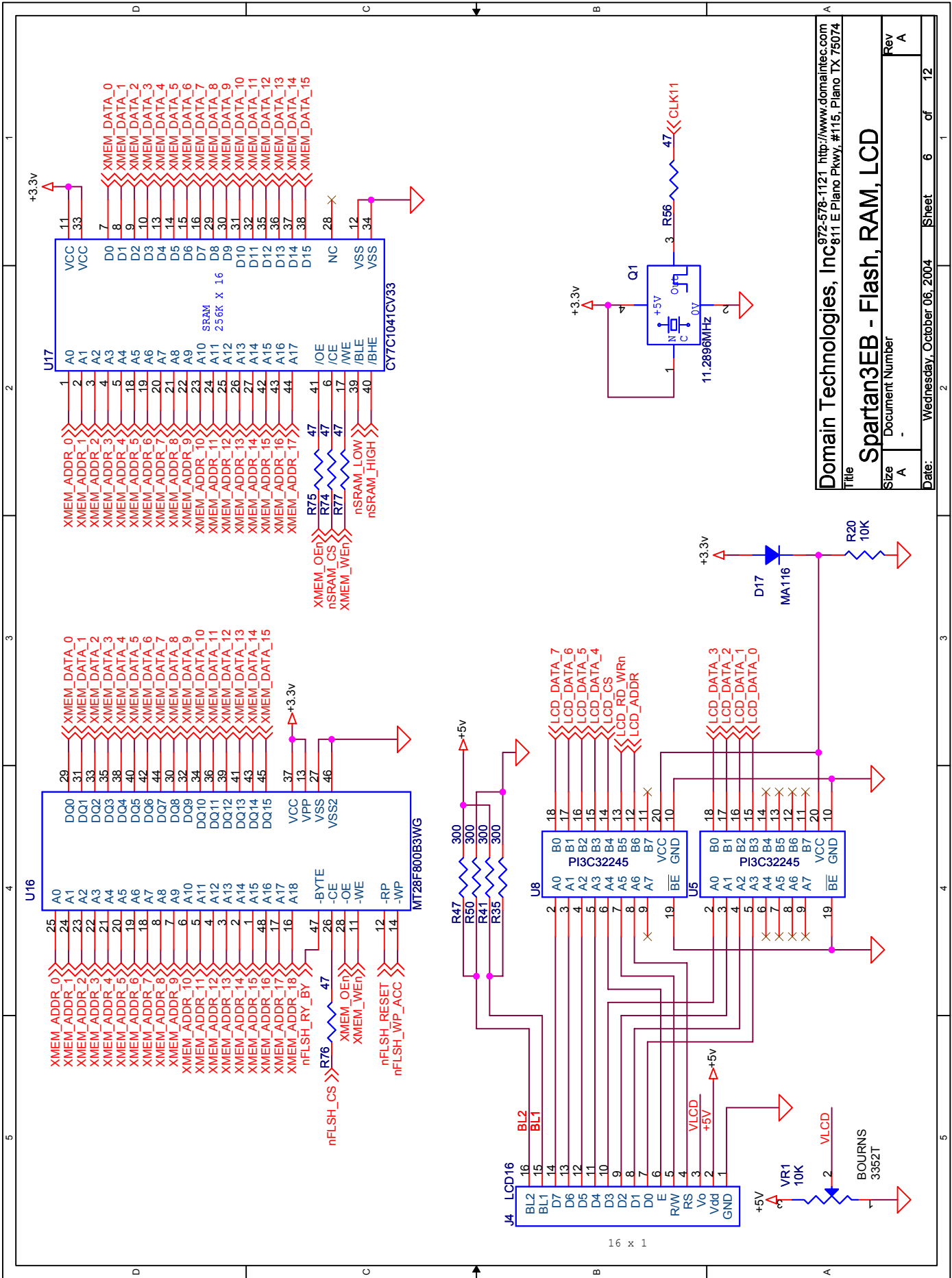
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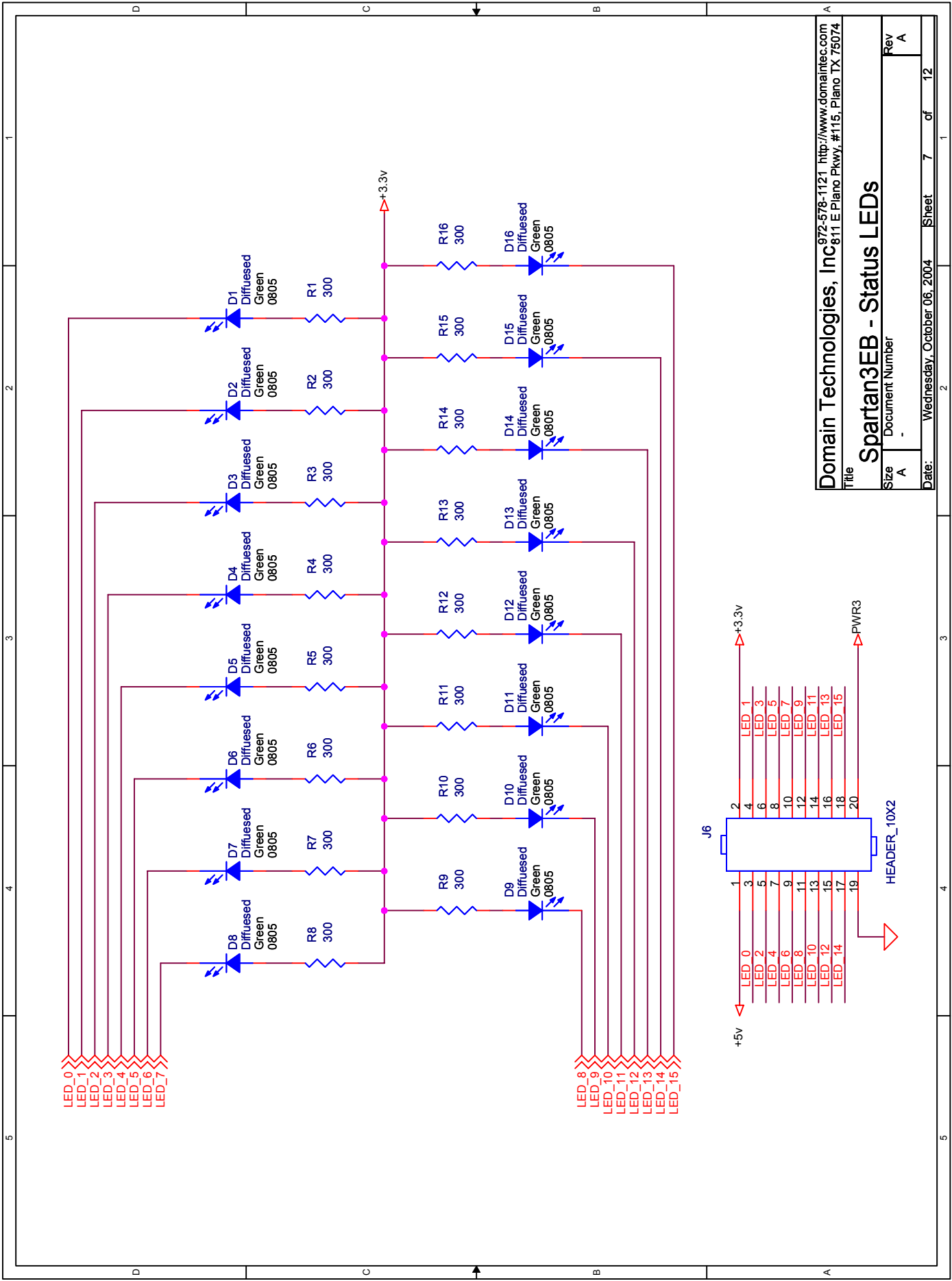
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**Spartan3EB - Flash, RAM, LCD**

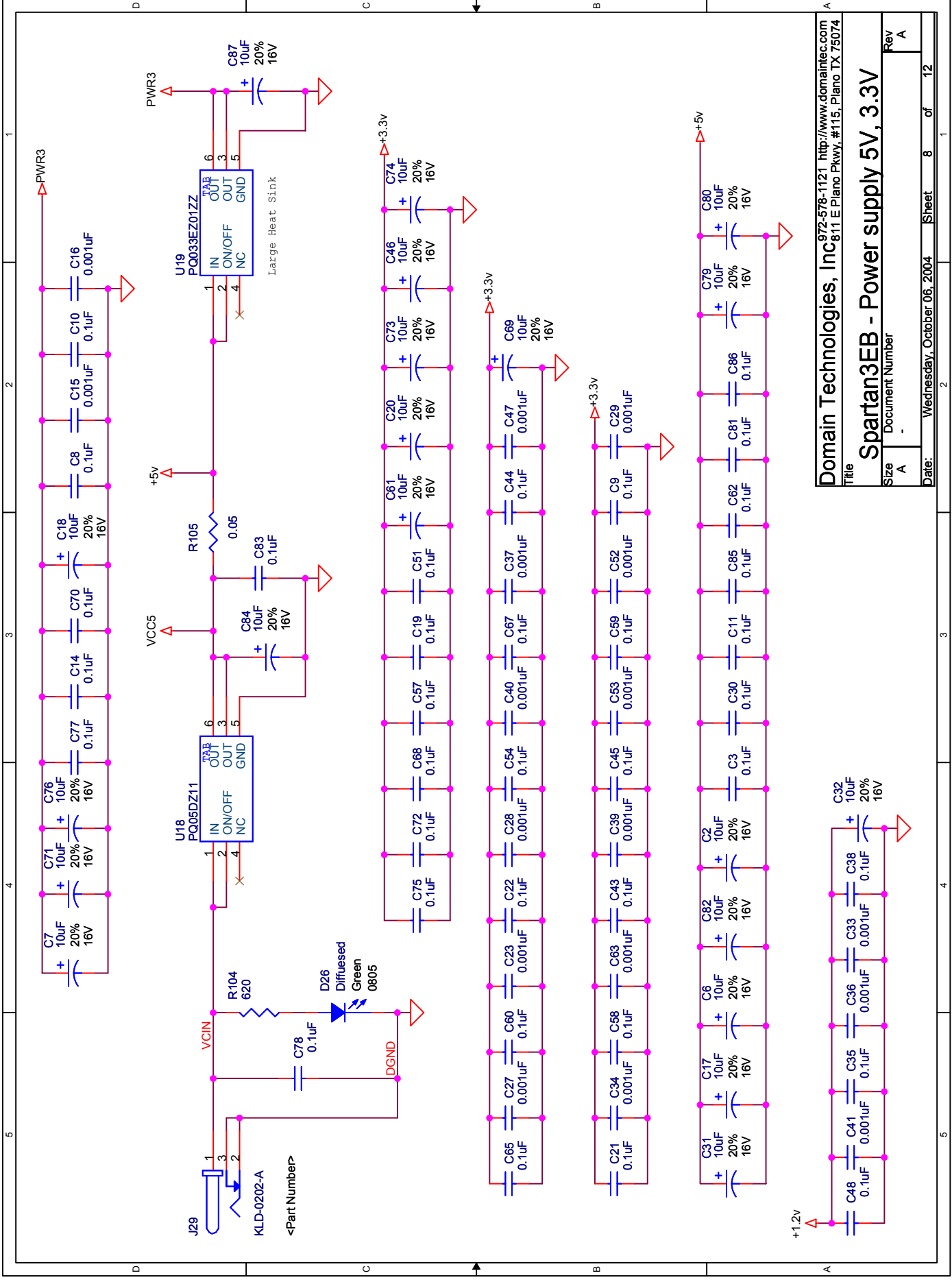
Document Number

Rev A

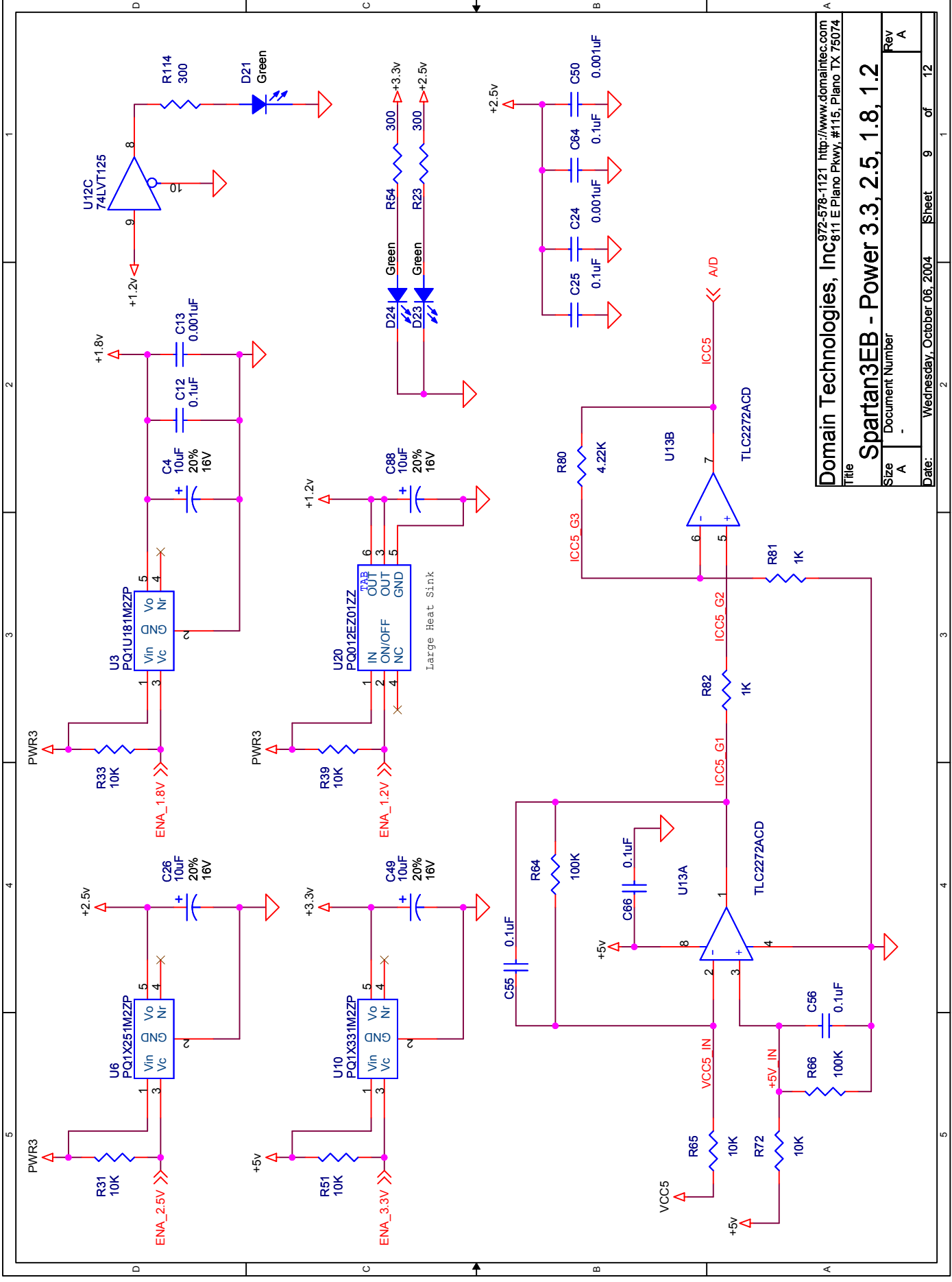
Date: Wednesday, October 06, 2004 Sheet 6 of 12



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| Title: Spartan3EB - Status LEDs                                                                                                                 |                  |
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| Date: Wednesday, October 06, 2004                                                                                                               | Rev: A           |
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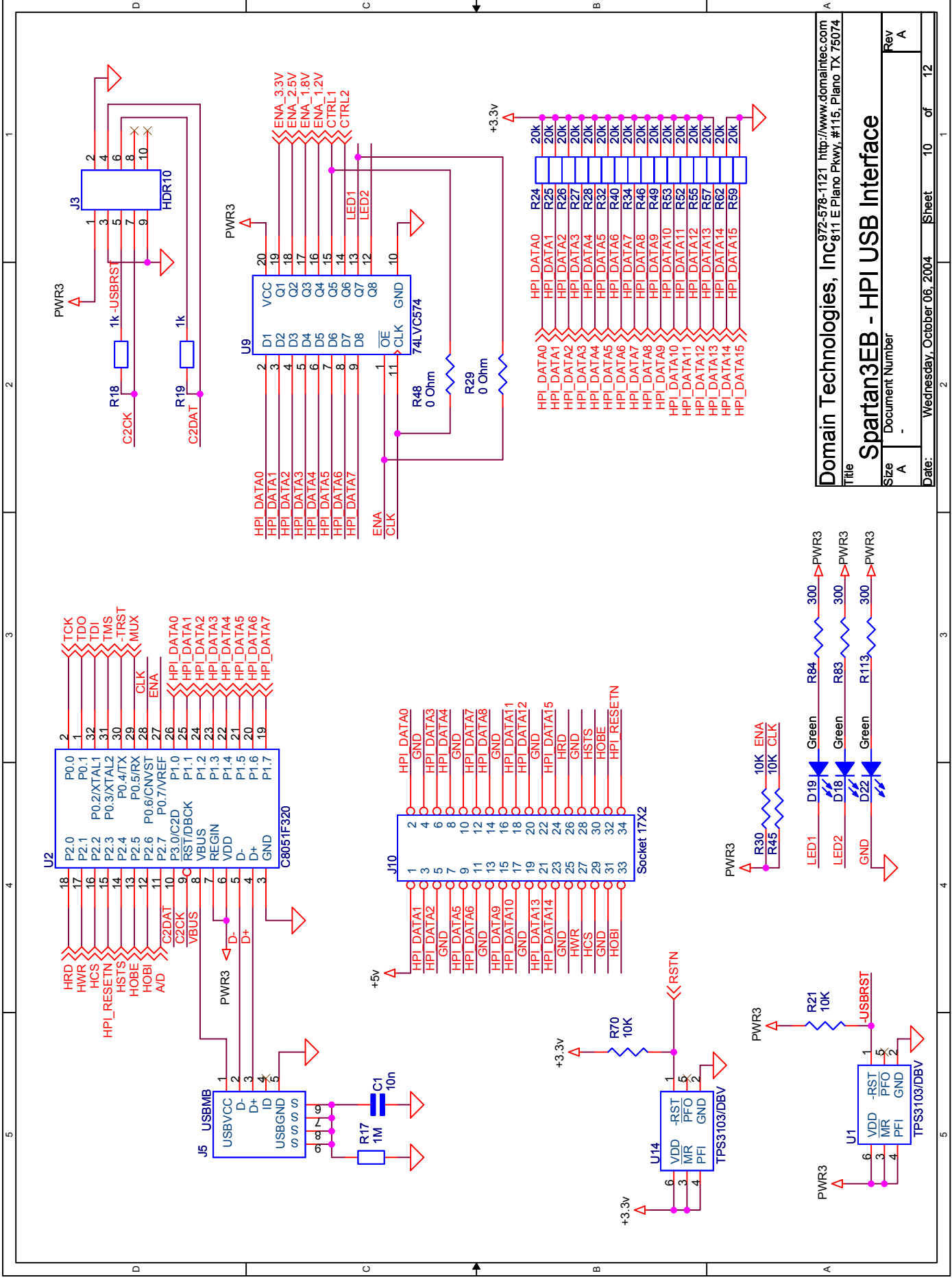


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| file Spartan3EB - Power supply 5V, 3.3V                                                               |                 |
| Size A                                                                                                | Document Number |
| Rev A                                                                                                 |                 |
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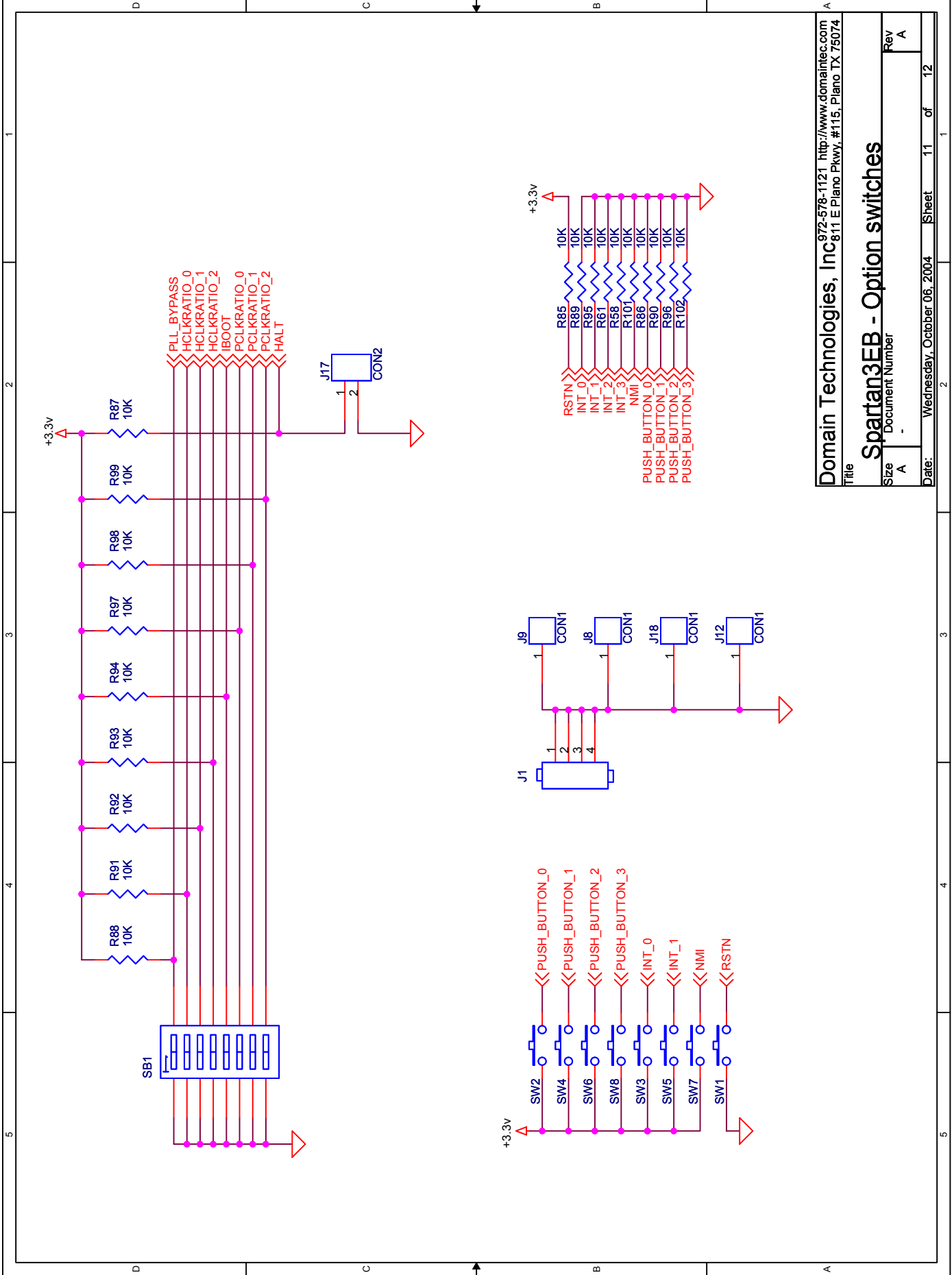


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| Size  | Document Number             | 811 E Plano Pkwy, #115, Plano TX 75074                                                                |         |
| Rev   | A                           |                                                                                                       |         |
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## Spartan3EB - Power 3.3, 2.5, 1.8, 1.2



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| <b>Spartan3EB - HPI USB Interface</b>                                                                 |                             |
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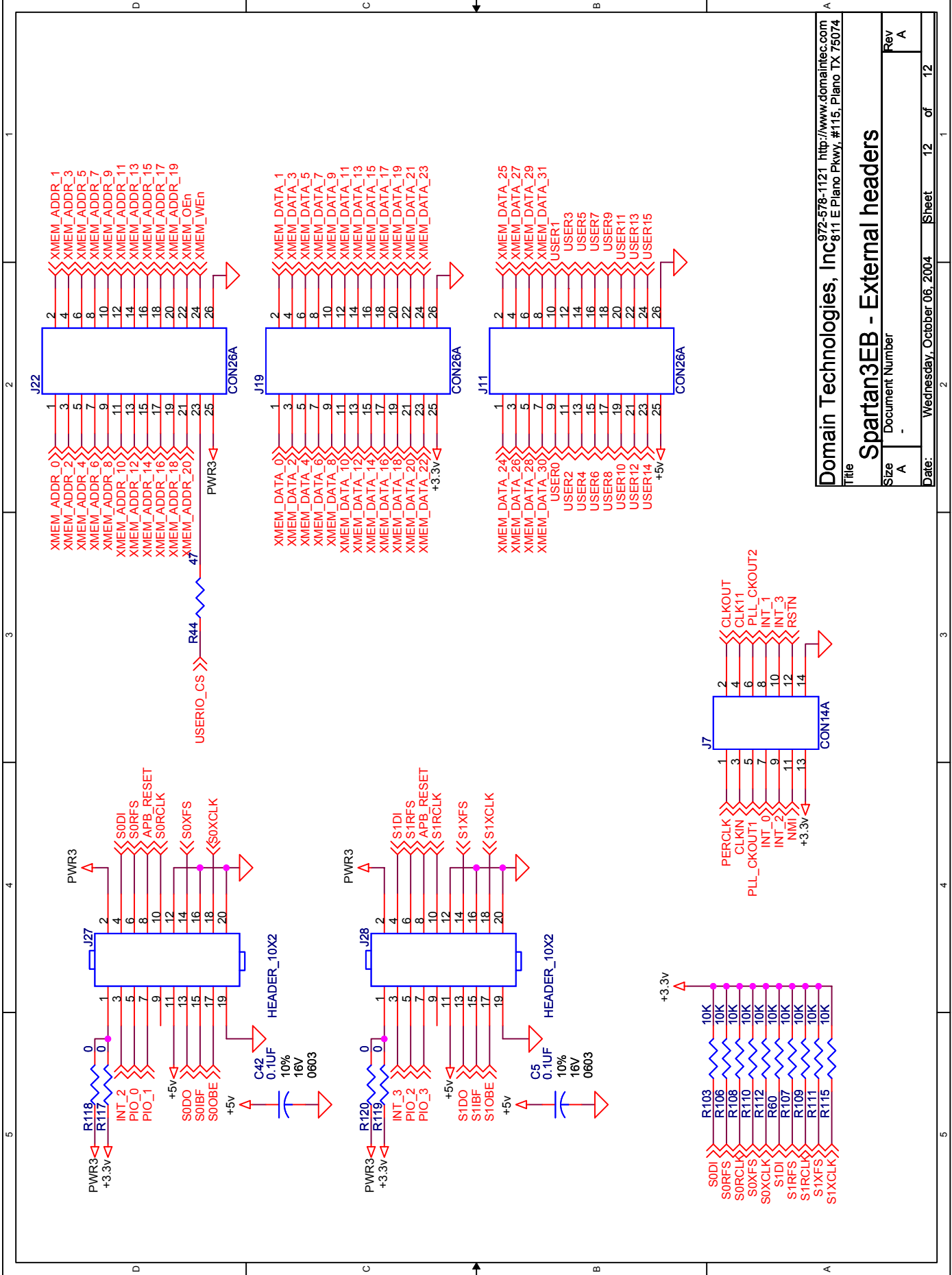


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Title: **Spartan3EB - Option switches**

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| Spartan3EB - External headers |                             |
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| Date:                         | Wednesday, October 06, 2004 |
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