

DSP*Card*-C31



TMS320C31 floating point DSP Card

A Product of Domain Technologies, Inc.

DSPCard-C31
User's Guide,
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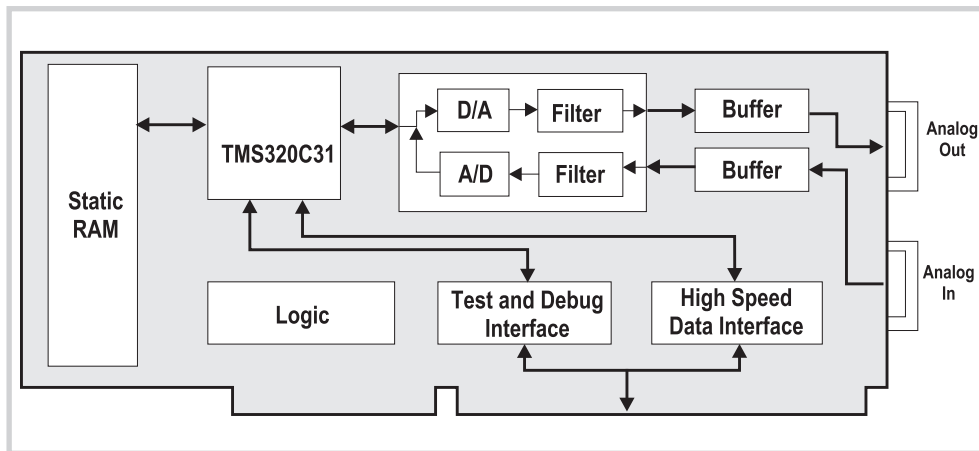
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CHAPTER 1 - Product Overview



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DSPCard-C31 is a general purpose Digital Signal Processing card based on the TMS320C31 floating-point DSP chip. The card is designed for the IBM PC computers and compatibles. The card is comprised four blocks: (1) The DSP, (2) The analog I/O, (3) Memory, (4) Interfaces to the PC.

1.1 - The TMS320C31 processor

The heart of the card is the industry standard floating point TMS320C31 Digital Signal Processor. The 'C31 processor has a rich instruction set, an integer/floating-point ALU, a 24 bit address bus, 2K words of internal memory, and a 64 word cache.

1.2 - The analog Input/Output

The analog Input/Output unit is comprised of an Analog Interface Chip (AIC), analog buffers, and two RCA jacks. The AIC chip has 14 bits resolution, sampling rates up to 19,200 samples per second, a built-in anti-aliasing filter, and a built-in smoothing filter. The AIC chip is programmed by the DSP.

1.3 - Memory

Memory is 32 bit wide zero wait state static RAM.

1.4 - Interfaces to the PC

DSPCard-C31 has two interfaces to the PC: a debugger interface and a high speed data transfer interface. The debugger interface is used by the loader and the debugger to perform such functions as loading an application program, setting breakpoints, running the DSP, single stepping, examining the DSP's resources, etc. The high-speed interface is a 16 bit bi-directional bus used for real-time data transfers between the DSP and the host PC.

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CHAPTER 2 - General Information

2.1 - Package Contents

- DSPCard-C31
- User's manual
- 3½" diskette

2.2 - Description of Supplied Files

Program files:

LDR_C30.EXE Loader program, it runs on the PC

RST_C30.EXE Reset program, it runs on the PC

PC to DSP interface example files:

TEST_C31.ASM Test program, it runs on the DSP

TEST_C31.OBJ Test program, it runs on the DSP

TEST_PC.C Test program, it runs on the PC

TEST_PC.EXE Test program, it runs on the PC

TEST_PC.BAT Batch file to start the above programs

DSP to debugger interface example files:

TEST_IO.ASM Test program, it runs on the DSP

TEST_IO.OBJ Test program, it runs on the DSP

TEST_IO.CMD Macro command file for TEST_IO.ASM

TEST_IO.DAT Example data file

2.3 - Operating Environment

DSPCard-C31 resides inside an IBM PC or compatible computer (16 bit ISA type slot).

2.4 - IBM PC Requirements

The minimum IBM-PC requirements are:

- 16 bit ISA slot

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2.5 - Hardware Installation

1. DSPCard-C31 resides in the Host PC's I/O address space. The four dip switches are used to set the base address of the card. Four settings are possible, thus up to four cards can be installed simultaneously inside a PC. Table 2-1 shows the switch settings with the respective I/O address range.
2. Install the card inside the PC's chassis.

I/O Range	SW1-1	SW1-2	SW1-3	SW1-4	
0x240-0x25f	ON	ON	ON	OFF	Default
0x280-0x29f	ON	OFF	ON	OFF	
0x320-0x33f	OFF	ON	ON	OFF	
0x340-0x35f	OFF	OFF	ON	OFF	

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2.6 - Software Installation

No software installation is required, just copy the supplied files to a hard drive directory.

2.7 - DSPCard-C31 versus TMS320C30 EVM

Domain Technologies' DSPCard-C31 is very similar to Texas Instruments' TMS320C30 EVM card. Table below summarizes the differences between the two cards.

	TMS320C30 EVM	DSPCard-C31
Processor	TMS320C30	TMS320C31
Processor clock	30 MHz	33 MHz
Memory	16 K	32 K, 128 K, or daughter card expansion
AIC's master clock	Uses the DSP's oscillator: 5.00 MHz	Independent oscillator: 5.184MHz
AIC's nominal sampling rate	7.716 kHz	8 kHz
LED	No LED	Monitoring LED connected to XF1
DSP's Secondary bus	Used for PC communications	Not available, primary bus is used for PC communications
PC bus	8 bit	16 bit

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CHAPTER 3 - Interface Details

3.1 - DSP to AIC interface

The AIC chip interfaces directly to the C31's serial port. The AIC's master clock is generated by a dedicated crystal oscillator. The crystal can be changed by the user to accommodate for non-standard sampling rates. Table below details the connections between the AIC and the DSP.

DSPSignal	AICSignal
CLKXO	SCLK
DXO	DX
FSXO	\FSX
CLKRO	SCLK
DRO	DR
FSRO	\FSR
XFO	\RESET
TCLKO(not used)	*****
*****	MCLK (from oscillator)

The crystal installed on the board has a frequency of 5.184 MHz. With this frequency, the A/D and D/A sampling rates are:

7200 samples/sec
8000 samples/sec
9600 samples/sec
14400 samples/sec
19200 samples/sec

The DSP's serial port may be disconnected from the AIC and used for a different purpose. The 20 pin header available on DSPCard-C31 allows the installation of user designed daughter cards.

3.2 - AIC to RCA Interface

Analog Signal In:

The analog signal into the card is buffered before it is fed into the AIC chip. A two stage amplifier is provided for this purpose. The first stage is used for isolation, it is non-inverting, high-impedance with unity gain. The second stage is used to provide amplification, the gain factor is two. A wide selection of devices such as a microphone, a tape deck, CD player, or a signal generator may be connected directly into the input RCA connector. Please do not overdrive the input.

3

Maximum input voltage into RCA	± 1.5 V
--------------------------------	-------------

Maximum input voltage into AIC	3.0 V
--------------------------------	-------

Analog Signal Out:

The analog signal out of the AIC chip is buffered before it is outputted to the RCA jack. The buffer is single stage power amplifier with a gain of four. Since the amplifier is a power amplifier, low impedance speakers(4, 8, or 16 ohms) can be connected directly to the output RCA connector. Other devices such as a tape deck, an active speaker, an oscilloscope, or an audio amplifier may also be connected directly to the output RCA connector.

RCA Output Load	RCA Output clipping voltage
4 Ohm load	± 3.5 V
8 Ohm load	± 6.5
16 Ohm load	± 10.0 V

AIC Output load	AIC Output clipping voltage
High impedance	± 2.5 V

3.3 - DSP to Memory Interface**3**

The DSP's memory is 32 bit wide high speed static RAM. Up to 128K words may be installed on the card. Headers are provided to allow further memory expansion. The following are the different memory configurations:

Size of memory	Location of memory chips
32K x 32 bit	On board
128K x 32 bit	On board
over 128K x 32 bit	On board with a daughter card

3.4 - Debugger Interface (PC to DSP)

The PC interfaces with the DSP through the dedicated debug and test port available on the TMS320C31. This dedicated debug and test port is used by the loader and debugger software to perform such functions as: load a DSP program, set breakpoints, run the DSP, examine memory, single-step, etc. A special purpose chip called the Test Bus Controller Chip (TBC: part # SN74ACT8990) provides the protocol interface between the PC and the DSP chip. The loader program provided with DSPCard-C31 uses this test and debug port to load application programs into the C31 chip.

3.5 - High Speed Interface (PC to DSP)

The high speed interface between the PC and the DSP is a bi-directional 16 bit interface. The interface is comprised of two bi-directional buffers (74ALS652) with control and decoding logic. Driver software for the PC and the DSP sides is supplied with this card.

CHAPTER 4 - Software Description

4.1 - Loader Program (LDR_C30.EXE)

LDR_C30.EXE loads an application program into the DSP and runs the application program. -P is a switch that defines the base address of the DSP card. The default address is 0x240. The following are a few examples:

LDR_C30 -P=240 TEST.OUT (Load card at 0x240)

LDR_C30 -P=280 TEST.OUT (Load card at 0x280)

LDR_C30 TEST.OUT (Load card at 0x240)

4.2 - Reset Program (RST_C30.EXE)

RST_C30.EXE resets the DSP. -P is a switch that defines the base address of the DSP card. The default address is 0x240. The following are a few examples:

RST_C30 -p=240 (Reset card at 0x240)

RST_C30 -p=280 (Reset card at 0x280)

RST_C30 (Reset card at 0x240)

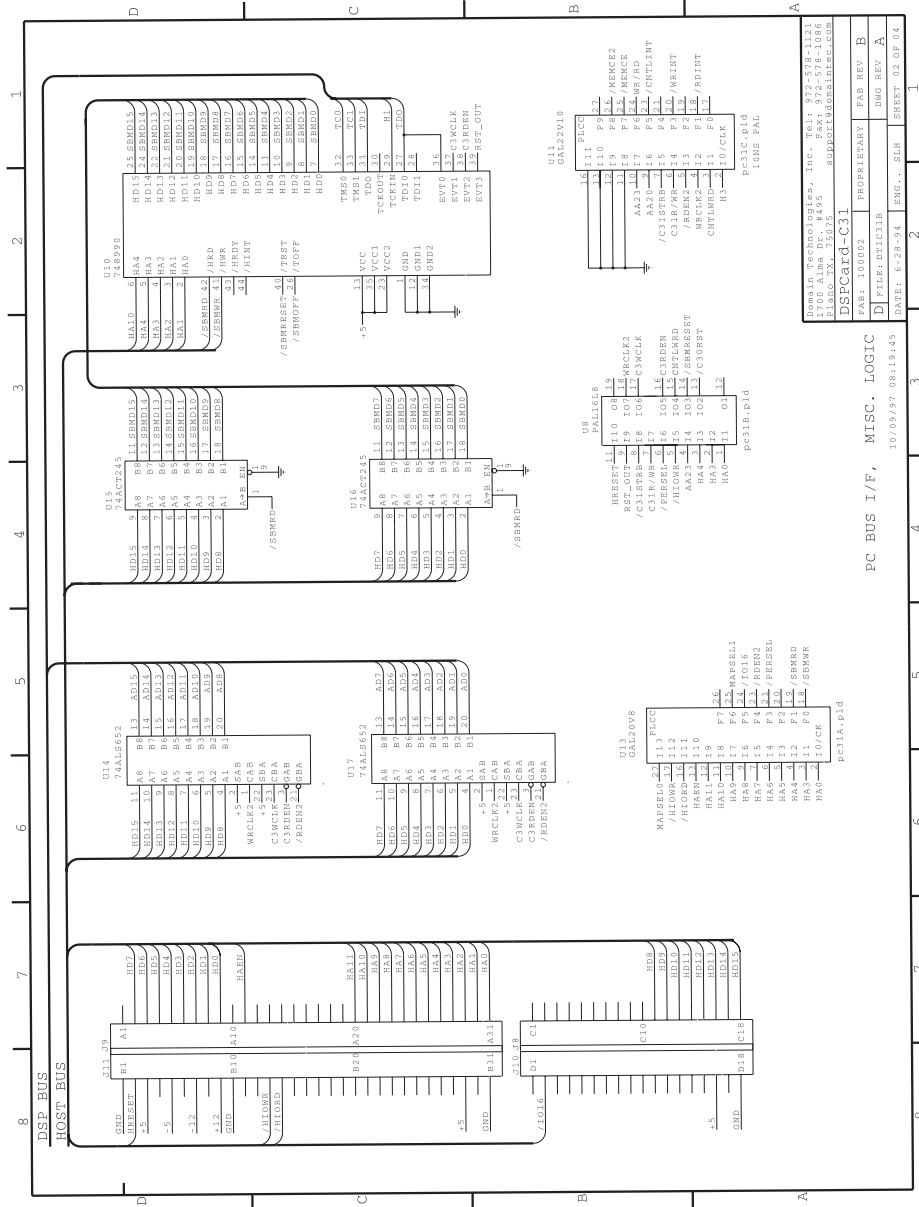
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4.3 - Example Programs

The example programs are supplied with the card.

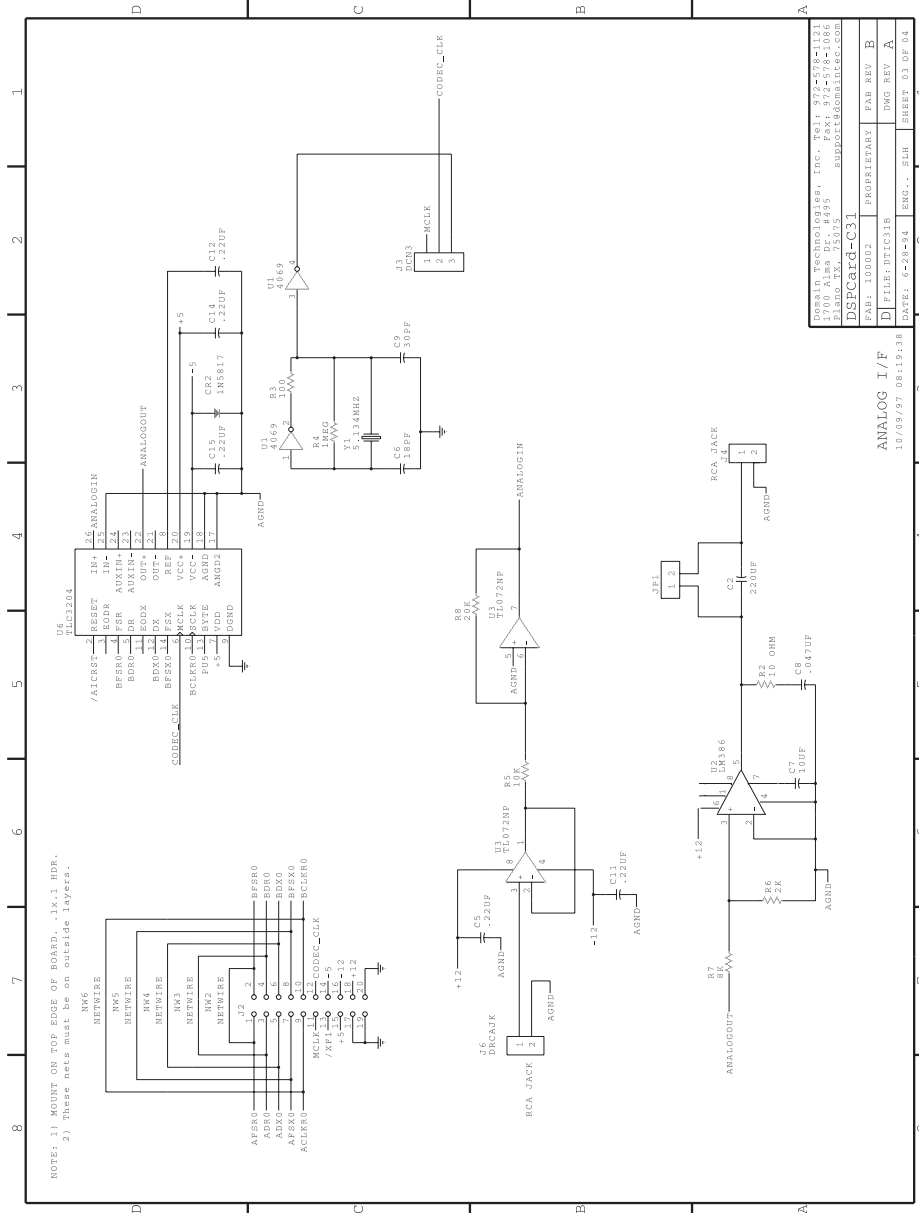
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5.2 - ISA interface

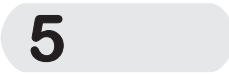


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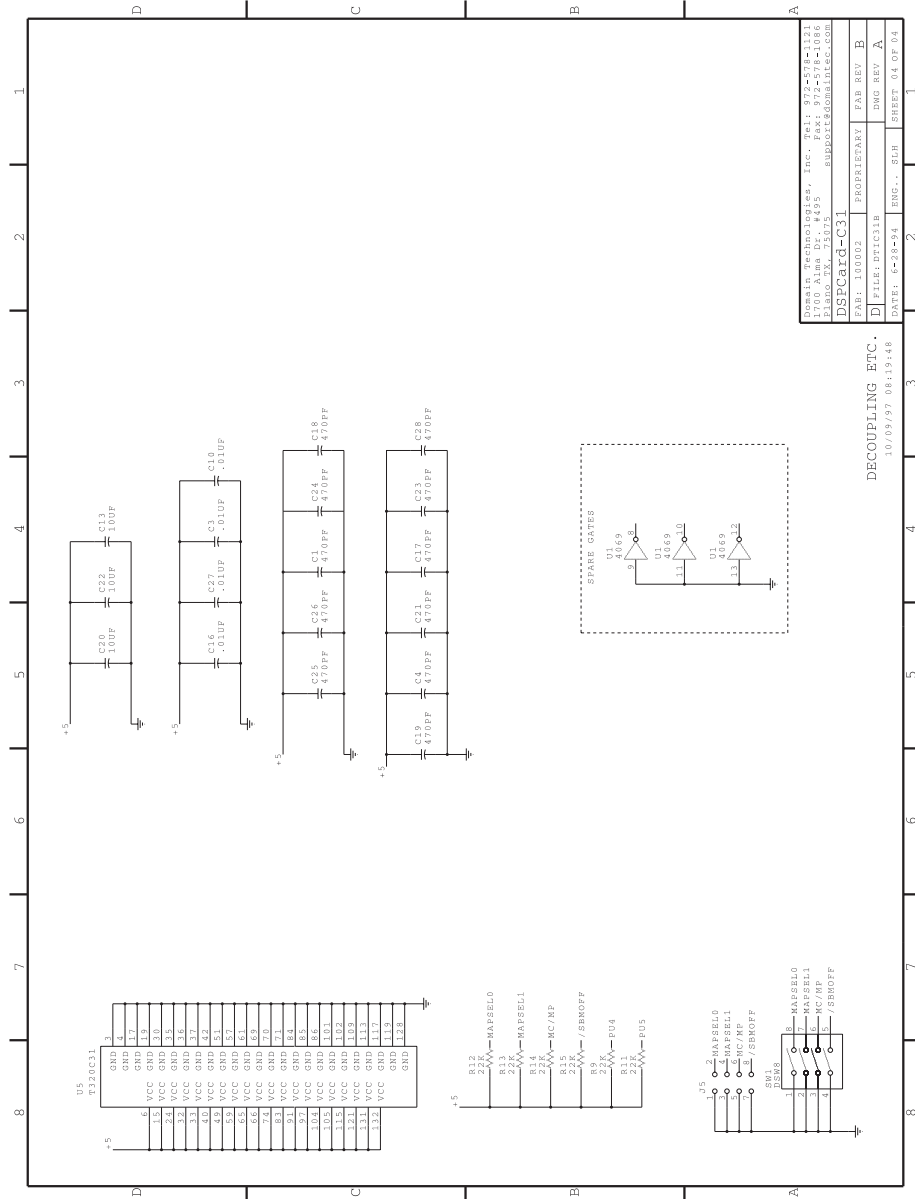
5.3 - Audio interface



TEXAS INSTRUMENTS, INC. P.O. BOX 6555, DALLAS, TX 75263 1700 ALBRITTON DRIVE, FARMERSVILLE, TX 77834 TEL: 972-792-2000 FAX: 972-792-1086 TEL: 512-792-2000 FAX: 512-792-1086 WWW.TI.COM	
DSPCard-C31	
FAB: 100002	PROPRIETARY
FILE: DTIC31B	DWG REV: A
DATE: 6-28-94	SHEET: 03 OF 04



5.4 - Switch and capacities



D		1	
D		2	
D		3	
D		4	
D		5	
D		6	
D		7	
D		8	

DECOUPLING ETC.
10/09/97 108:15:46

1700 Alpha Dr., #495
Bismarck, ND 58503
972-578-1000
972-578-1006
ESP@PERFORMANCE.COM

DSPCard-C31
ENG. 10/09/97 PROPRIETARY
DATE: 6-28-94
SHEET 04 OF 04

Device A (U13)

```

Name           PC31a;
date           7/7/94;
revision       C;
company        Domain Technologies;
assembly       pc31;
location       U13;
device         g20V8lcc;

PIN [2..7]     = HAO, [HA3..HA7];
PIN [9..14]    = [HA8..HA11], HAEN, GND;
PIN [16..17]   = HIORD, !HIOWR;
PIN [25]       = MAPSEL1;
PIN [27]       = MAPSELO;

PIN [18..21]   = !SBMWR, !SBMRD, BOARDSEL, !PERSEL;
PIN [23..24]   = !RDEN2, !IO16;

/* PC BUS Input ADDRESS BITS & IO RANGE SELECTION */
FIELD ADDR=[HA11..HA3];
FIELD IOSEL=[MAPSEL1..MAPSELO];
SBMSEL  = !HAEN & ADDR:[25F..240] & IOSEL:[0]
          # !HAEN & ADDR:[65F..640] & IOSEL:[0]
          # !HAEN & ADDR:[29F..280] & IOSEL:[1]
          # !HAEN & ADDR:[69F..680] & IOSEL:[1]
          # !HAEN & ADDR:[33F..320] & IOSEL:[2]
          # !HAEN & ADDR:[73F..720] & IOSEL:[2]
          # !HAEN & ADDR:[35F..340] & IOSEL:[3]
          # !HAEN & ADDR:[75F..740] & IOSEL:[3];

SBMRD        = SBMSEL & HIORD & !HA0;

SBMWR        = SBMSEL & HIOWR & !HA0;

RDEN2        = PERSEL & HIORD & !HA4 & !HA0;

IO16         = BOARDSEL; /* all accesses are 16 bit */
IO16.OE      = BOARDSEL; /* Use as tri-state output */

BOARDSEL     = PERSEL /* any access to the board */
              # SBMSEL;

```

```
PERSEL      = !HAEN & ADDR:[A5F..A40] & IOSEL:[0]
             # !HAEN & ADDR:[A9F..A80] & IOSEL:[1]
             # !HAEN & ADDR:[B3F..B20] & IOSEL:[2]
             # !HAEN & ADDR:[B5F..B40] & IOSEL:[3];
```

Device B (U8)

```

Name          PC31b;
date          7/7/94;
revision      A;
company       Domain Technologies;
assembly      pc31;
location      U8
device        gl6v8;

/* Inputs */

PIN [1..6]    = HA0, HA3, HA4, AA23, !HIOWR, !PERSEL;
PIN [7..11]   = C31R_W, !C31STRB, RST_OUT, GND, HRESET;

/* Outputs */

PIN [13..15] = !C30RST, !SBMRESET, CNTLWRD;
PIN [16..18] = C3RDEN, !C3WCLK, !WRCLK2;

C30RST        = RST_OUT
               # HRESET;

SBMRESET      = HRESET
               # PERSEL & HA4 & HA3 & HIOWR;

CNTLWRD       = PERSEL & !HA4 & !HA3 & !HA0;

C3RDEN        = C31R_W&C31STRB & AA23; /* ANY READ OF HIGH MEMORY */

C3WCLK        = !C31R_W&C31STRB & AA23; /* ANY WRITE TO HIGH MEMORY */

WRCLK2        = PERSEL & !HA4 & HA3 & !HA0 & HIOWR /* DATA */
               # PERSEL & !HA4 & !HA3 & !HA0 & HIOWR; /* CNTL WORD */

```

Device C (U11)

```

Name          PC31c;
date          7/7/94;
revision      A;
company       Domain Technologies;
assembly      pc31;
location      U11;
device        P22V10;

/* Inputs */
PIN [2..5]    = H3, CNTLWRD, !WCLK2, !RDEN2;
PIN [6..7]    = C31RWR, !C31STRB;
PIN [9..10]   = AA20, AA23;

/* Outputs */
PIN [17..18]  = RDINTS0, RDINTS1;
PIN [19..20]  = WRINTS0, WRINTS1;
PIN [22..23]  = CNTLINTS0, CNTLINTS1;
PIN [24..26]  = !WRRD, !MEMCE, !MEMCE2;

/* Define 3 separate state machines */

FIELD CNTLINT_SEQ = [CNTLINTS1, CNTLINTS0];
FIELD WRINT_SEQ   = [WRINTS1, WRINTS0];
FIELD RDINT_SEQ   = [RDINTS1, RDINTS0];

/* State definitions, common for all 3 state machines. */

$define        IDLE 3 /* WAITING FOR INT SOURCE ACTIVE */
$define        IRDY 2 /* WAITING FOR INT SOURCE !ACTIVE */
$define        INTS1 1 /* INTERRUPT OUT LOW 2 CLOCK */
$define        INTS0 0 /* INTERRUPT OUT LOW 1 CLOCK */

SEQUENCE      WRINT_SEQ {
    PRESENT IDLE
    IF (WCLK2 & !CNTLWRD)      NEXT IRDY;
    IF (!WCLK2 # CNTLWRD)      NEXT IDLE;

```

```
PRESENT IRDY
IF WCLK2          NEXT IRDY;
IF CNTLWRD       NEXT IDLE;
IF (!WCLK2 & !CNTLWRD)  NEXT INTS0;

PRESENT          INTS0
NEXT INTS1;

PRESENT          INTS1
NEXT IDLE;
}

SEQUENCE CNTLINT_SEQ {
PRESENT IDLE
IF (WCLK2 & CNTLWRD)  NEXT IRDY;
IF (!WCLK2 # !CNTLWRD)  NEXT IDLE;

PRESENT IRDY
IF WCLK2          NEXT IRDY;
IF !WCLK2        NEXT INTS0;

PRESENT          INTS0
NEXT INTS1;

PRESENT          INTS1
NEXT IDLE;
}

SEQUENCE RDINT_SEQ {
PRESENT IDLE
IF (RDEN2 & !CNTLWRD)  NEXT IRDY;
IF (!RDEN2 # CNTLWRD)  NEXT IDLE;

PRESENT IRDY
IF (RDEN2 & !CNTLWRD)  NEXT IRDY;
IF CNTLWRD          NEXT IDLE;
IF (!RDEN2 & !CNTLWRD)  NEXT INTS0;
```

```
PRESENT      INTS0
             NEXT INTS1;

PRESENT      INTS1
             NEXT IDLE;
}

WRRD = C31RWR;          /* INVERTED IN PIN DEFINITIONS */

/* MEMORY IS A23 LOW, PERIPHIALS A23 HIGH */
/* Onboard memory when A20 LOW. ( 0FFFFFF..00000 ) */
/* Actual range with 128k x 8 rams ( 1FFFFF..00000 ) */

MEMCE = !AA23 & !AA20 & C31STRB;

/* MEMORY IS A23 LOW, PERIPHIALS A23 HIGH */
/* Expansion memory when A20 HIGH. ( 7FFFFFF..100000 ) */
/* Actual range with 128k x 8 rams ( 11FFFFF..100000 ) */

MEMCE = !AA23 & AA20 & C31STRB;
```