Domain Technologies, incorporated in 1991, offers over 10 years of experience in the field of emulation and debug tools for a wide variety of industry standard and proprietary 8, 16, 24, and 32-bit microcontroller, RISC, and DSP architectures.

Our products are a vital part of your company’s DSP development infrastructure! We are committed to improving the efficiency of embedded software development for our customers. Providing emulators and evaluation boards as well as boundary scanning and debugging software, our products promote cost reduction through time-to-market savings. Utilize our comprehensive debugging tools in conjunction with our boards for scalable and flexible testing of single DSPs, multiple DSPs, local access to multiple devices, and remote access to multiple devices.

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1 Introduction

Use the A3P-MRAM development module when designing and developing your microcontroller applications. The A3P-MRAM FPGA module supports designing and developing of customized SL8051 (Silicon Laude) or Core8051 (Actel) microcontroller applications. As shown above, the board features an Actel ProASIC3 re-programmable FPGA, 512 kbytes of non-volatile Magnetoresistive Random Access Memory (MRAM), thirty-four undedicated user I/O's, with configurable voltage level between 1.5 and 3.3V, and an on-board USB-JTAG interface for programming the device as well as debugging the resulting microcontroller application.

1.1 Package Contents

The A3P-MRAM board ships with the following:
- USB Cable
- Installation CD with Users Guide

1.2 Features

The A3P-MRAM has the following features:
Re-programmable Actel ProASIC3 A3P1000 or A3P250, Flash Based, FPGA
- 512 kbytes 35ns Non-volatile MRAM
- 4 User LEDs
- 2 push button switches
- Up to 40 User I/Os
- Integrated USB-JTAG Interface
- USB-powered with External 5 Volt Option
- Dimensions 2.4" x 1"
1.3 Related Components
Use Domain Technologies BoxView IDE in conjunction with the A3P-MRAM’s JTAG interface to the FPGA, allowing for device reprogramming and debugging of the loaded processor core. Domain Technologies also has the A3P-MRAM-BASE board to provide a prototype area for circuit development. For more information contact Domain Technologies or review www.domaintec.com.

2 Installation
Included with the A3P-MRAM is a USB cable and installation CD. Verify they have been delivered with the module. The installation CD contains a control application for programming the FPGA. Insert the installation CD into your CD ROM drive. If auto detect is enabled in your system environment setup, then the installation program will automatically launch. Otherwise, double-click the A3PMRAMinstall.exe file located on the CD drive from within Windows Explorer. Follow the steps through the program to perform the installation of the A3P-MRAM supporting software.

3 A3P-MRAM Board Functionality
The A3P-MRAM is a stand-alone multi-purpose controller module. It features a re-programmable FPGA, which can be programmed with the Silicon Laude SL8051 or Actel Core8051 microcontroller. The external 512 KB of MRAM allows for non-volatile storage of the controller data. The user program loaded on the module will always be available on power-up. The MRAM allows for very fast writing and read back of the contents; this provides an advantage over Flash memory which requires very long programming cycles.

- Quad LEDs providing simple status display.
- Two pushbutton momentary switches.

The microcontroller has direct control of four 8-bit bidirectional GPIO ports and single RS-232 port without transceiver for optional serial port logic which could be implemented on the FPGA. The built-in USB microcontroller provides a JTAG interface to the FPGA, allowing for device reprogramming and debugging of the loaded processor core. This functionality is compatible
with Domain Technologies BoxViewIDE and Actel's SoftConsole development system for Core8051.

The A3P-MRAM is available with the re-programmable Actel ProASIC3 A3P1000 or A3P250 FPGA. The module is also available without MRAM installed. The module is shipped with the SL8051 from Silicon Laude programmed. The test application loaded in the MRAM writes to I/O ports testing pin connections. This can be verified with the A3P-MRAM-BASE board, where the LEDs will scroll.

## 4 A3P-MRAM Initialization

The A3P-MRAM module can be initialized either with the BoxView IDE, BoxView or a3pinit.exe utility. In BoxView debugger there is a command STAPL, which will reprogram device: `STAPL -a action progFile.stp`

The action could be: read_idcode, program, verify or erase.

The a3pinit.exe executes similar operation, using the parameters passed on the command line: `a3pinit.exe -A action progFile.stp`

Sample programming session:

```
C:\Actelprj\SL8051_A3pMram\designer\impl1>a3pinit -aprogram SL8051.stp
a3pinit.exe v. 1.00 - A3P FPGA programming utility
(c) 2007, Domain Technologies, Inc. [Jul 10 2007]
Opening connection to: A3P-MRAM
usbemumot 1.10.48 [Aug 27 2007] [1400] [000007] Rev B
alg version in file = 14
DirectC version = 17
IDCODE = 2c281cf
Erase ...
Erase 21.938
Programming FPGA Array
Program 4500/0 1:19.969, 56.278 rps
Verifying FPGA Array
Verify 4500/0 1:10.937, 63.442 rps
Exit code = 0 - Success
Elapsed time = 2:52.468
```
5 A3P-MRAM JTAG test

The USB-JTAG controller could be used for the basic functionality test. The JTAG port is used to reprogram the A3P FPGA device. It can be also used to interface to the user’s logic by way of the user JTAG block. The built-in microcontroller can also to access a secondary JTAG port. This allows to create custom JTAG interface. To test main JTAG port there is provided test utility: EmuTest.exe.
The picture above shows results after selecting A3P-MRAM, Open and Read
Idocde. The first number represents A3P1000 idcode, and second one is a
device ID of the programmed SL8051 microcontroller.
The low level JTAG operations are available through the “Advanced JTAG
operations”. The “Streaming” feature is not supported on A3P-MRAM.
The built-in microcontroller supports also various custom interfaces to the
FPGA logic, which could be used for the real-time data transfer between host
PC and the FPGA module.
6 Appendix A: Schematics

Top of A3P-MRAM

Bottom of A3P-MRAM